VCU110 Evaluation Board

User Guide

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VCU110 Evaluation Board Features

Overview

The VCU110 evaluation board for the Xilinx Virtex® UltraScale™ XCVU190-2FLGC2104E FPGA provides a hardware environment for developing and evaluating designs targeting the UltraScale XCVU190-2FLGC2104E FPGA. The VCU110 evaluation board provides features common to many evaluation systems, including QDRII+ and RLD3 component memory, a hybrid memory cube component memory, a CFP4 Quad C form-factor pluggable module connector, an Ethernet PHY, general purpose I/O, a four-lane PCI Express® interface connector, and two UART interfaces. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to two high pin count (HPC) FMC connectors.

See Appendix H, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the VCU110 board.

VCU110 Evaluation Board Features

The VCU110 evaluation board features are listed here. Detailed information for each feature is provided in Feature Descriptions.

- Virtex UltraScale XCVU190-2FLGC2104E FPGA
- 144 Mb QDRII+ component memory interface (1 x 18-bit SIO device)
- 2 x 576 Mb RLD3 component memories (1 x 36-bit x 16M), 1 x 18-bit x 32M CIO devices)
- 4 GB Hybrid Memory Cube (HMC)
- Dual 512 Mb Quad-SPI (QSPI) flash memory
- Micro secure digital (SD) connector
- USB JTAG interface through Digilent module with micro-B USB connector
- Clock sources:
  - SI5335A Quad clock generator
  - Si570 IIC programmable LVDS clock generator
  - Three SI5328 clock multiplier and jitter attenuators

    - SMA user clock connector pair (differential)
- 52 GTY transceivers (13 Quads)
    - 5 Quads connected to Interlaken connector
    - 2 Quads connected to 2 BullsEye™ SMA connectors
    - 2 Quads connected to EXAMAX connector
    - 4 Quads connected to CPF4 connector
- 52 GTH transceivers (13 Quads)
    - 8 Quads connected to HMC
    - 2 Quads connected to FMC HPC0 connector DP
    - 2 Quads connected to FMC HPC1 connector DP
    - 1 Quad connected to PCIe® cable connector
- Ethernet PHY SGMII interface with RJ-45 connector
- Dual USB-to-UART bridge with micro-B USB connector
- Status LEDs
- User I/O (pushbuttons, DIP switch, LEDs)
- Pmod header
- Two VITA 47.1 FMC HPC connectors
- Configuration options:
    - Quad-SPI flash memory
    - USB JTAG configuration port (Digilent module)
    - Platform cable 2 mm 2x7 shrouded header J3 JTAG configuration port
- Zynq® XC7Z010 based system controller

Block Diagram

The VCU110 evaluation board block diagram is shown in Figure 1-1.

The VCU110 board schematics are available for download from the Xilinx Virtex UltraScale FPGA VCU110 Evaluation Kit website. The page numbers shown in Figure 1-1 refer to schematic page numbers in the VCU110 schematic XTP407.

CAUTION! *The VCU110 evaluation board can be damaged by electrostatic discharge (ESD). Follow ESD prevention measures when handling the board.*

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.
- If a wrist strap is not available, ground yourself by touching the metal chassis before handling the adapter or any other part of the computer/server.

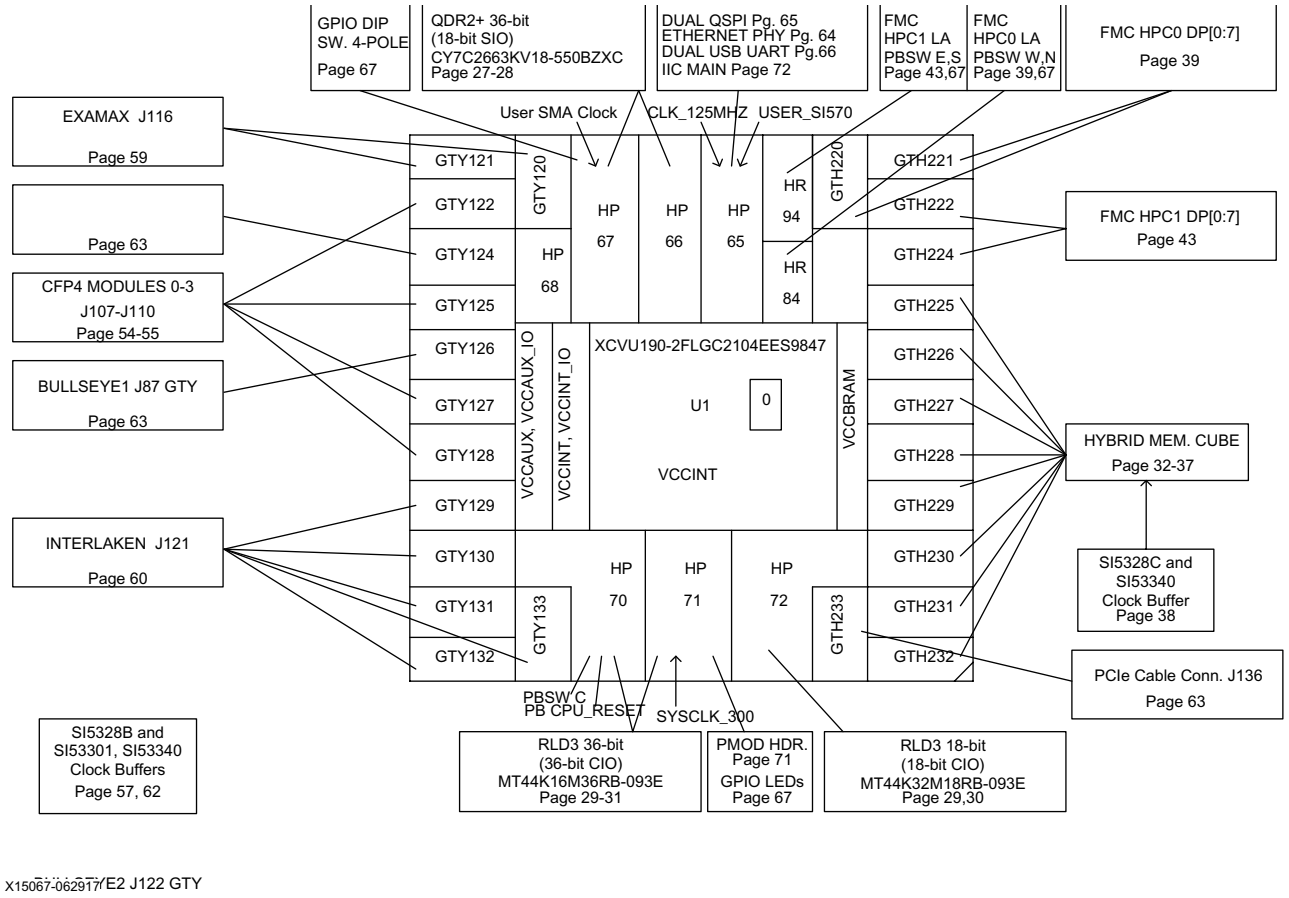

Figure 1-1: **VCU110 Evaluation Board Block Diagram**

Board Layout

Figure 1-2 shows the VCU110 evaluation board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1. Detailed information is provided under Feature Descriptions.

IMPORTANT: *The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.*

CAUTION! *The VCU110 evaluation board can be damaged by electrostatic discharge (ESD). Follow ESD prevention measures when handling the board.*

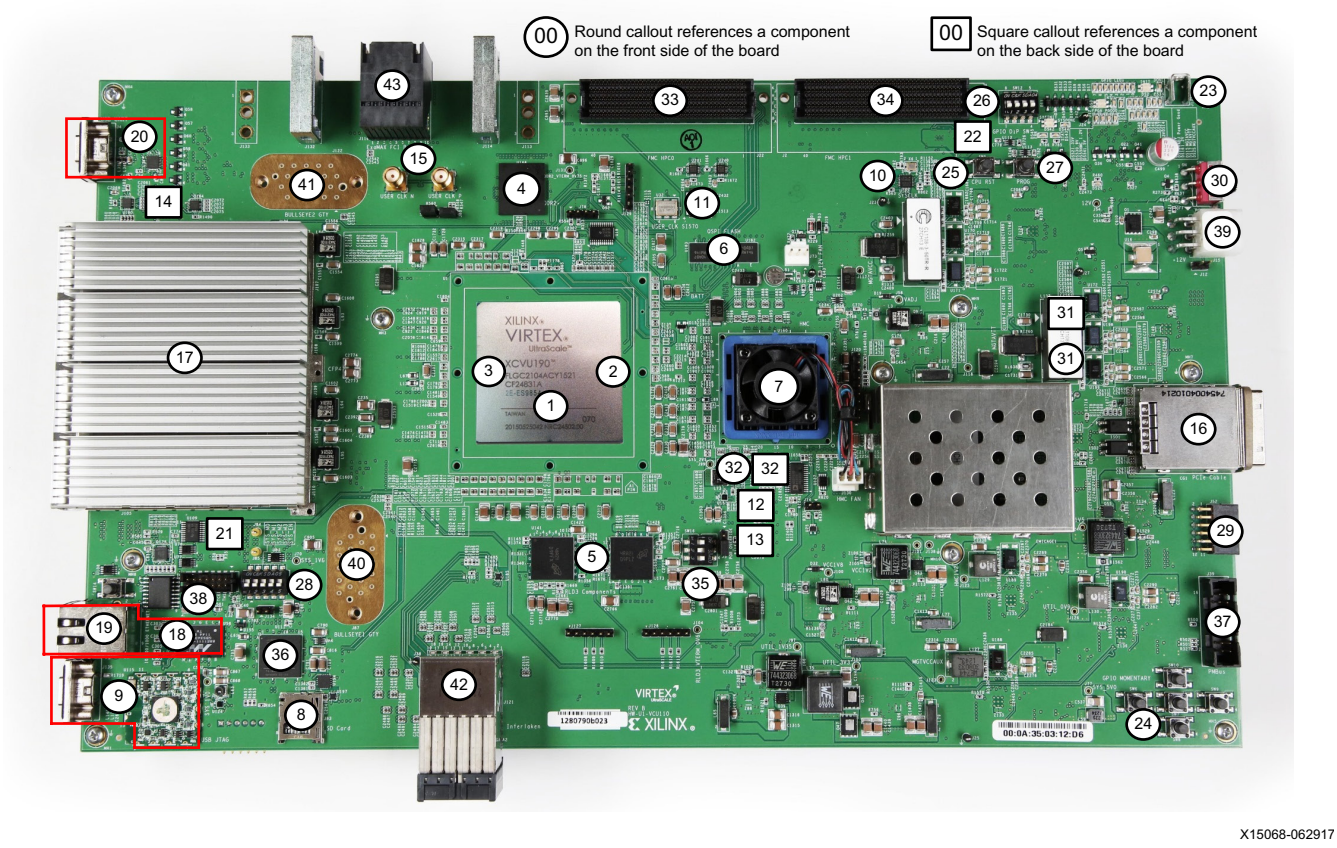

Figure 1-2: **VCU110 Board Component Locations**

Table 1-1: **VCU110 Board Component Descriptions**

Callout	Feature	Notes	Schematic 0381556 Page Number
1	Virtex UltraScale XCVU190-2FLGC2104E FPGA, (U1) (with fan-sink on soldered FPGA)	XCVU190-2FLGC2104E, COFAN 30-5530-03	
2	GTY Transceivers, 13 Quads	Embedded within FPGA U1	9-12
3	GTH Transceivers, 13 Quads	Embedded within FPGA U1	13-16
4	QDR2+ Component Memory, 576 Mb 18-bit QDR2+ SIO component memory I/F (U168)	Cypress CY7C2663KV18-550BZXC	26
5	RLD3 Component Memory, RLD3 36-bit and 18-bit component memory I/F (U141, U173)	Micron MT44K16M36RB-093E Micron MT44K32M18RB-093E	28-29
6	Dual Quad-SPI Flash Memory (128Mb) (U114)	Micron N25Q128A11ESF40G	62
7	2 GB Hybrid Memory Cube (HMC) (U160) (with fan-sink)	Micron MT43A4G40200NFA, RADIAN XLX027	31-36
8	Micro-SD Card Interface connector (J83)	Molex 5025700893	56
9	USB JTAG Interface (U115), w/Micro-B connector	Digilent USB JTAG module	25

Table 1-1: **VCU110 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic 0381556 Page Number
10	System Clock. multi-output clock generator, SYSCLK and other clocks, 1.8V LVDS (U122)	SI5335A-B02436-GM, 4 outputs: 300 MHz, 125 MHz, 90 MHz, 33.33 MHz	46
11	Programmable User Clock, I2C programmable user clock LVDS (U32) with 1-to-2 LVDS buffer (U32)	Silicon Labs SI570BAB0000544DG (default 156.250MHz) with Si53340 buffer	47
12	Jitter-Attenuating Clock Multipliers for HMC jitter attenuated clock (U57)	Silicon Labs SI5328B-C-GMR	37
13	Jitter-Attenuating Clock Multipliers for ExaMAX jitter attenuated clock (U181)	Silicon Labs SI5328C-C-GM	59
14	Jitter-Attenuating Clock Multipliers for CFP4 module jitter attenuated clock (U179)	Silicon Labs SI5328C-C-GM	55
15	User SMA Clock source, user differential SMA clock P/N (J34/J35)	Rosenberger 32K10K-400L5	60
16	PCIe Cable Connector, (J136), with cage (CG1)	J136 Molex 0755860010 CG1 Molex 0745400401	60
17	CFP Module Quad Connectors (CFP4), (J108-J110)	4x Yamaichi CN121S-056-0001	52-53
18	10/100/1,000Mb/s Tri-Speed Ethernet PHY w/RJ45, SGMII mode only, (U58,P3)	Marvell M88E1111-BAB1C000 with Halo HFJ11-1G01E-L12RL RJ45	61
19	Ethernet PHY Status LEDs, LEDs are integrated into P3 bezel	Halo HFJ11-1G01E-L12RL RJ45 integrated status LEDs (Rev B)	61
20	Dual USB-to-UART Bridge, bridge device (U34) with mini-B connector (J4)	Silicon Labs CP2105-F01-GM bridge, Hirose ZX62D-AB-5P8 connector	63
21	I2C Bus, Topology and Bus Switches, I2C Bus MUX (U28)	TI TCA9548APWR	69
22	I2C Bus, Topology and Bus Switches, I2C Bus MUX (U80)	TI PCA9544ARGYR	69
23	User GPIO LEDs, (DS6-DS10, DS31-DS33)	GPIO LEDs, green 0603 Lumex SML-LX0603GW-TR	64
24	User Pushbuttons, active-High (SW6-SW10)	E-Switch TL3301EF100QG in North, South, East, West, Center pattern	64
25	CPU Reset Pushbutton, user CPU reset, active-High (SW5)	E-Switch TL3301EF100QG	64
26	GPIO DIP Switch, (SW12)	4-pole C&K SDA04H1SBD	64
27	Program_B Pushbutton Switch, FPGA PROG pushbutton (SW4)	E-Switch TL3301EF100QG	64
28	System controller mode DIP switch, DIP switch (SW15) See Switches and Appendix C, Getting Started with System Controller	5-pole C&K SDA05H1SBD	51

Table 1-1: **VCU110 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic 0381556 Page Number
29	User PMOD GPIO Header, PMOD header (J52) w/level-shifters (U41)	2x6 0.1 inch male header Sullins PBC36DAAN; TI TXS0108EPWR	68
30	Power On/Off Slide Switch SW1	C&K 1201M2S3AQE2	71
31	VCU110 Board Power System, power management system (top and bottom)	Maxim MAX15301 and MAX15303 digital POL controllers	72-86
32	Monitoring Voltage and Current, power management voltage and current sensing SYSMON external circuitry (top and bottom)	Analog Devices MUX ADG707BRUZ TI op amps INA333AIDGKR	66-67
33	FMC HPC0 Connector J22	Samtec ASP_134486-01	38-41
34	FMC HPC1 Connector J2	Samtec ASP_134486-01	42-45
35	Mode DIP switch (SW16) see FPGA Configuration	3-pole C&K SDA03H1SBD	3
36	VCU110 Zynq-7000 SoC XC7Z010 System Controller (U111)	XC7Z010CLG225	48-50
37	2x8 shrouded PMBus connector (J39), see Monitoring Voltage and Current	Assman AWHW16G-0202	70
38	2x7 2 mm shrouded JTAG cable connector (J3) See USB JTAG Interface	MOLEX 87832-1420	25
39	12V power input 2x6 connector (J15). See Power On/Off Slide Switch SW1	MOLEX 39-30-1060	71
40	Samtec BULLSEYE1 Connector (J87)		60
41	Samtec BULLSEYE2 Connector (J122)		60
42	Interlaken Connector (J121)	TYCO 2187194	58
43	ExaMAX Backplane Connector, (J116)	FCI 10126363-101LF	57

Notes:

1. The VCU110 board schematics are available for download from the VCU110 Evaluation Kit website.
2. The VCU110 board jumper header locations are shown in Figure A-1.

Feature Descriptions

Virtex UltraScale XCVU190-2FLGC2104E FPGA

[Figure 1-2, callout 1]

The VCU110 board is populated with the Virtex UltraScale XCVU190-2FLGC2104E FPGA. For further information on Virtex UltraScale FPGAs, see *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893)*Virtex UltraScale Architecture Data Sheet* (DS893), [Ref 1].

FPGA Configuration

The VCU110 board supports two of the five UltraScale FPGA configuration modes:

- Master SPI using the onboard dual Quad SPI (QSPI) flash memory
- JTAG using either:
  - USB JTAG configuration port (Digilent module U115), or
  - Xilinx platform cable, 2 mm, keyed flat cable header (J3)

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW16 positions 1, 2, and 3 respectively as shown in Figure 1-3. The FPGA default mode setting M[2:0] = `101`, selecting the JTAG configuration mode.

Table 1-2: **VCU110 Board FPGA Configuration Modes**

Configuration Mode	SW16 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master SPI	`001`	x1, x2, x4	Output
JTAG	`101`	x1	Not applicable

For full details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

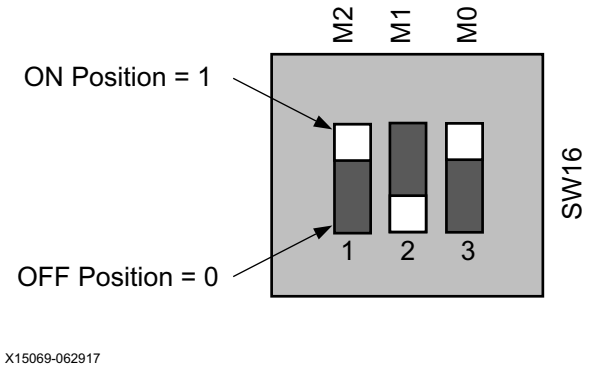

Figure 1-3: **SW16 Default Settings**

Encryption Key Backup Circuit

The XCVU190 FPGA U1 implements bitstream encryption key technology. The VCU110 board provides the encryption key backup battery circuit shown in Figure 1-4. The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCVU190 FPGA U1 V_{CCBATT} pin AN13. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the SYS_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and a 4.7 kΩ current limiting resistor. The nominal charging voltage is 1.42V.

Figure 1-4 shows the encryption key battery backup circuit.

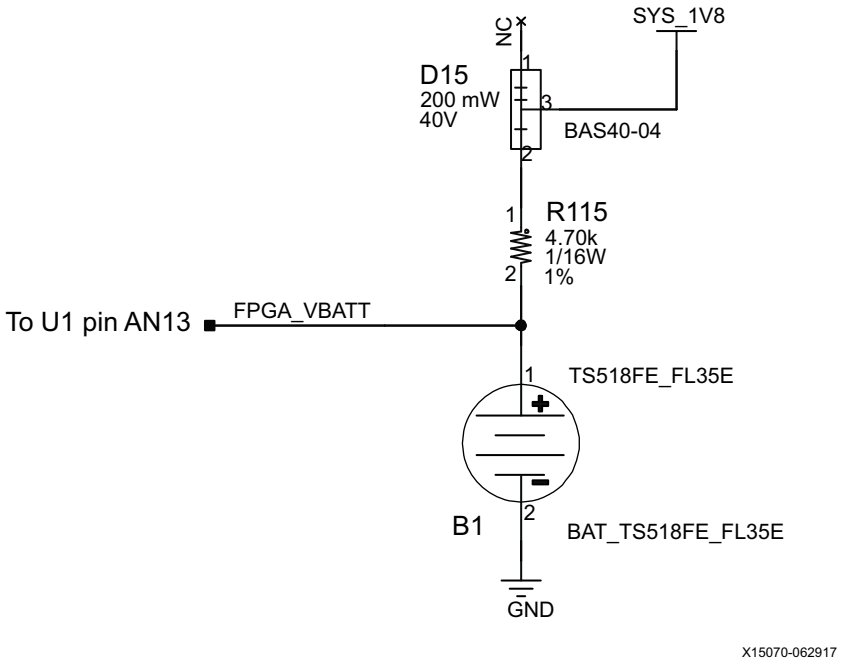

Figure 1-4: **Encryption Key Backup Circuit**

I/O Voltage Rails

There are eight I/O banks available on the XCVU190 device and the VCU110 board. The voltages applied to the FPGA I/O banks (shown in Figure 1-5) used by the VCU110 board are listed in Table 1-3.

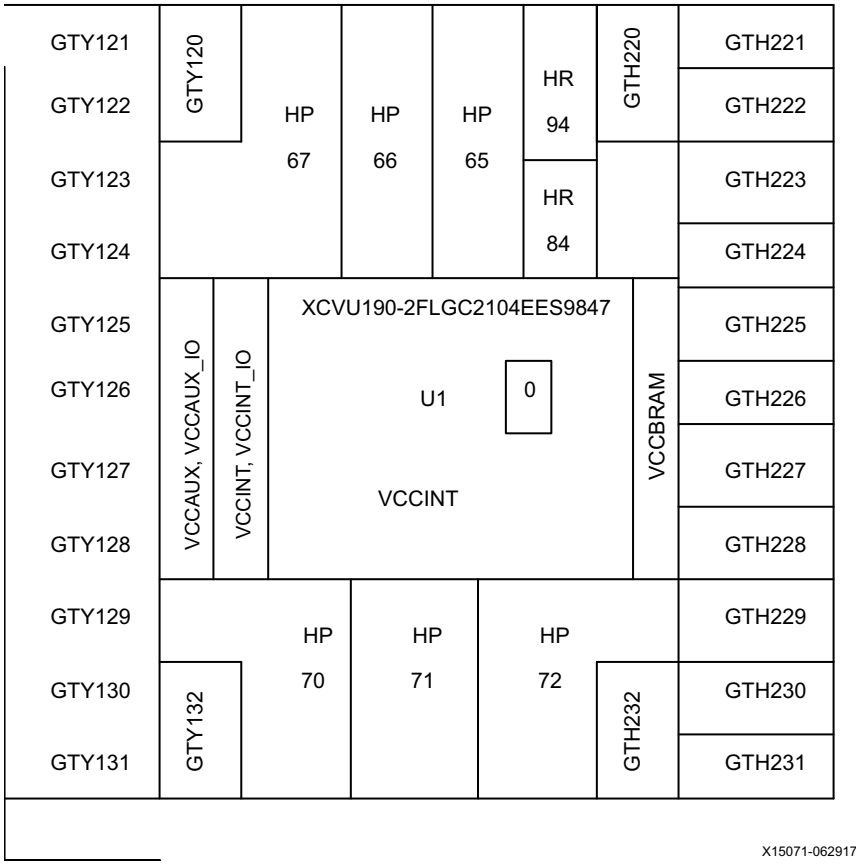

Figure 1-5: **UltraScale XCVU190 Bank Locations**

Table 1-3: **I/O Bank Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8_FPGA	1.8V
HP Bank 65	VCC1V8_FPGA	1.8V
HP Bank 66	VCC1V5_FPGA	1.5V
HP Bank 67	VCC1V5_FPGA	1.5V
HP Bank 68	VADJ_1V8_FPGA	1.8V
HP Bank 70	VCC1V2_FPGA	1.2V
HP Bank 71	VCC1V2_FPGA	1.2V
HP Bank 72	VCC1V2_FPGA	1.2V
HR Bank 84	VCC1V8_FPGA	1.8V
HR Bank 94	VCC1V8_FPGA	1.8V

QDR2+ Component Memory

[Figure 1-2, callout 4]

The 144 Mb QDR2+ component memory system is comprised of one 18-bit separate I/O (SIO) device located at U168:

- Manufacturer: Cypress
- Part number: CY7C2663KV18-550BZXC synchronous pipelined SRAM
- Configuration: Four-word burst architecture with on-die termination (ODT)
  - 144 Mb: 8Mb x 18, with read cycle latency of 2.5 cycles
- Supply voltage: 1.8V
- Datapath width: 18 bits, supports separate independent read and write data ports
- Data rate: Data transferred at 1100 MHz with 550 MHz clock

The VCU110 XCVU190 FPGA QDR2+ interface performance is documented in the *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893)[Ref 1].

This memory system is connected to the XCVU190 HP banks 66 and 67. The DDR4 0.75V V_{TT} termination voltage (net QDR2_VTERM_0V75) is sourced from TI TPS51200DR linear regulator U167. The connections between QDR2 component memory U168 and XCVU190 banks 66 and 67 are listed in Table 1-4.

Table 1-4: **QDR2 Memory U168 18-bit SIO I/F to FPGA U1 Banks 66 and 67**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin Number	Pin Name
AM23	QDR2_18B_D0	HSTL_I_DCI	P10	D0
AM24	QDR2_18B_D1	HSTL_I_DCI	N11	D1
AN23	QDR2_18B_D2	HSTL_I_DCI	M11	D2
AP22	QDR2_18B_D3	HSTL_I_DCI	K10	D3
AM26	QDR2_18B_D4	HSTL_I_DCI	J11	D4
AN25	QDR2_18B_D5	HSTL_I_DCI	G11	D5
AN26	QDR2_18B_D6	HSTL_I_DCI	E10	D6
AP25	QDR2_18B_D7	HSTL_I_DCI	D11	D7
AP23	QDR2_18B_D8	HSTL_I_DCI	C11	D8
AU26	QDR2_18B_D9	HSTL_I_DCI	B3	D9
AT26	QDR2_18B_D10	HSTL_I_DCI	C3	D10
AR25	QDR2_18B_D11	HSTL_I_DCI	D2	D11
AT24	QDR2_18B_D12	HSTL_I_DCI	F3	D12
AR24	QDR2_18B_D13	HSTL_I_DCI	G2	D13
AU22	QDR2_18B_D14	HSTL_I_DCI	J3	D14

Table 1-4: **QDR2 Memory U168 18-bit SIO I/F to FPGA U1 Banks 66 and 67 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin Number	Pin Name
AT22	QDR2_18B_D15	HSTL_I_DCI	L3	D15
AR22	QDR2_18B_D16	HSTL_I_DCI	M3	D16
AR23	QDR2_18B_D17	HSTL_I_DCI	N2	D17
BA22	QDR2_18B_A0	HSTL_I_DCI	A3	A0
AY24	QDR2_18B_A1	HSTL_I_DCI	A9	A1
AW23	QDR2_18B_A2	HSTL_I_DCI	B4	A2
AV24	QDR2_18B_A3	HSTL_I_DCI	B8	A3
AW22	QDR2_18B_A4	HSTL_I_DCI	C5	A4
BB24	QDR2_18B_A5	HSTL_I_DCI	C6	A5 (BL2/BL4)
BE23	QDR2_18B_A6	HSTL_I_DCI	C7	A6
BD23	QDR2_18B_A7	HSTL_I_DCI	N5	A7
BC23	QDR2_18B_A8	HSTL_I_DCI	N6	A8
BE24	QDR2_18B_A9	HSTL_I_DCI	N7	A9
BF22	QDR2_18B_A10	HSTL_I_DCI	P44	A10
BF21	QDR2_18B_A11	HSTL_I_DCI	P55	A11
BC24	QDR2_18B_A12	HSTL_I_DCI	P77	A12
BB23	QDR2_18B_A13	HSTL_I_DCI	P88	A13
BE22	QDR2_18B_A14	HSTL_I_DCI	R33	A14
BD22	QDR2_18B_A15	HSTL_I_DCI	R44	A15
BB22	QDR2_18B_A16	HSTL_I_DCI	R55	A16
BA24	QDR2_18B_A17	HSTL_I_DCI	R77	A17
BA25	QDR2_18B_A18	HSTL_I_DCI	R88	A18
AV23	QDR2_18B_A19	HSTL_I_DCI	R9	A19
AY25	QDR2_18B_A20	HSTL_I_DCI	A10	NC_72M
AY22	QDR2_18B_A21	HSTL_I_DCI	A2	NC_144M
AN24	QDR2_18B_BWS0_B	HSTL_I_DCI	B7	BWS0_BS0_B_B
AT25	QDR2_18B_BWS1_B	HSTL_I_DCI	A5	BWS1_BS1_B_B
AU23	QDR2_18B_K_P	DIFF_HSTL_I_D	B6	K
AU24	QDR2_18B_K_N	DIFF_HSTL_I_D	A6	K_B
AY23	QDR2_18B_WPS_B	HSTL_I_DCI	A7	WPS_B
BF24	QDR2_18B_RPS_B	HSTI_I	A8	RPS_B
AW25	QDR2_18B_DOFF_B	HSTL_I_DCI	H1	DOFF_B
AN28	QDR2_18B_Q0	HSTL_I_DCI	P11	Q0
AM29	QDR2_18B_Q1	HSTL_I_DCI	M10	Q1
AN29	QDR2_18B_Q2	HSTL_I_DCI	L11	Q2

Table 1-4: **QDR2 Memory U168 18-bit SIO I/F to FPGA U1 Banks 66 and 67 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin Number	Pin Name
AM31	QDR2_18B_Q3	HSTL_I_DCI	K11	Q3
AP28	QDR2_18B_Q4	HSTL_I_DCI	J10	Q4
AN31	QDR2_18B_Q5	HSTL_I_DCI	F11	Q5
AR27	QDR2_18B_Q6	HSTL_I_DCI	E11	Q6
AR29	QDR2_18B_Q7	HSTL_I_DCI	C10	Q7
AR30	QDR2_18B_Q8	HSTL_I_DCI	B11	Q8
AV29	QDR2_18B_Q9	HSTL_I_DCI	B2	Q9
AV28	QDR2_18B_Q10	HSTL_I_DCI	D3	Q10
AU29	QDR2_18B_Q11	HSTL_I_DCI	E3	Q11
AW26	QDR2_18B_Q12	HSTL_I_DCI	F2	Q12
AU28	QDR2_18B_Q13	HSTL_I_DCI	G3	Q13
AU27	QDR2_18B_Q14	HSTL_I_DCI	K3	Q14
AT29	QDR2_18B_Q15	HSTL_I_DCI	L2	Q15
AT27	QDR2_18B_Q16	HSTL_I_DCI	N3	Q16
AT31	QDR2_18B_Q17	HSTL_I_DCI	P3	Q17
AT30	QDR2_18B_CQ	HSTL_I_DCI	A11	CQ
AV26	QDR2_18B_CQ_B	HSTL_I_DCI	A1	CQ_B
NA	NA	NA	P6	QVLD

The VCU110 QDR2+ 18-bit SIO memory component interface adheres to the constraints guidelines documented in the QDRII+ Design Guidelines section of the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150) [Ref 3] for Vivado Design Suite. The VCU110 QDR2 memory component interface is a 40Ω impedance implementation.

For more details about the Cypress QDR2+ component memory, see the Cypress CY7C2663KV18-550BZXC data sheet [Ref 20].

RLD3 Component Memory

[Figure 1-2, callout 5]

The 1152 Mb RLD3 component memory system is comprised of two 576 Mb RLDRAM3 devices located at U141 and U173.

U141:

- Manufacturer: Micron
- Part number: MT44K16M36RB-093E

- Configuration: 576 Mb: 1 Mb x 36 x 16 banks
- Supply voltage: 1.35V
- Datapath width: 36 bits common I/O (CIO)
- Data rate: 1066 MHz DDR operation (2133 Mb/s/ball)

U173:

- Manufacturer: Micron
- Part number: MT44K16M18RB-093E
- Configuration: 576 Mb: 2 Mb x 18 x 16 banks
- Supply voltage: 1.35V
- Datapath width: 18 bits common I/O (CIO)
- Data rate: 1066 MHz DDR operation (2133 Mb/s/ball)

The VCU110 XCVU190 FPGA RLD3 interface performance is documented in the *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893) [Ref 1].

This memory system is connected to the XCVU190 HP banks 70, 71 and 72. The RLD3 0.6V V_{TT} termination voltage (net RLD3_VTERM_0V6) is sourced from TI TPS51200DR linear regulator U143. The connections between RLD3 component memory U141 and XCVU190 banks 70 and 71 are listed in Table 1-5.

Table 1-5: **RLD3 Memory U141 36-bit I/F to FPGA U1 Banks 70 and 71**

FPGA (U1) Pin	Schematic Net Name	I/O Standard
C27	RLD3_36B_DQ0	SSTL12
D29	RLD3_36B_DQ1	SSTL12
A29	RLD3_36B_DQ2	SSTL12
B27	RLD3_36B_DQ3	SSTL12
B26	RLD3_36B_DQ4	SSTL12
A28	RLD3_36B_DQ5	SSTL12
C28	RLD3_36B_DQ6	SSTL12
C29	RLD3_36B_DQ7	SSTL12
B28	RLD3_36B_DQ8	SSTL12
K29	RLD3_36B_DQ9	SSTL12
J26	RLD3_36B_DQ10	SSTL12
K28	RLD3_36B_DQ11	SSTL12
N27	RLD3_36B_DQ12	SSTL12
L28	RLD3_36B_DQ13	SSTL12
K26	RLD3_36B_DQ14	SSTL12

Table 1-5: **RLD3 Memory U141 36-bit I/F to FPGA U1 Banks 70 and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard
M27	RLD3_36B_DQ15	SSTL12
K27	RLD3_36B_DQ16	SSTL12
L29	RLD3_36B_DQ17	SSTL12
H27	RLD3_36B_DQ18	SSTL12
J27	RLD3_36B_DQ19	SSTL12
G26	RLD3_36B_DQ20	SSTL12
F29	RLD3_36B_DQ21	SSTL12
G28	RLD3_36B_DQ22	SSTL12
E27	RLD3_36B_DQ23	SSTL12
E29	RLD3_36B_DQ24	SSTL12
F26	RLD3_36B_DQ25	SSTL12
F28	RLD3_36B_DQ26	SSTL12
N29	RLD3_36B_DQ27	SSTL12
N32	RLD3_36B_DQ28	SSTL12
M30	RLD3_36B_DQ29	SSTL12
N30	RLD3_36B_DQ30	SSTL12
K31	RLD3_36B_DQ31	SSTL12
M32	RLD3_36B_DQ32	SSTL12
J32	RLD3_36B_DQ33	SSTL12
J31	RLD3_36B_DQ34	SSTL12
K32	RLD3_36B_DQ35	SSTL12
E28	RLD3_36B_DM0	SSTL12
L30	RLD3_36B_DM1	SSTL12
D26	RLD3_36B_QK0_P	SSTL12
D27	RLD3_36B_QK0_N	SSTL12
N28	RLD3_36B_QK1_P	DIFF_SSTL12
M28	RLD3_36B_QK1_N	DIFF_SSTL12
H28	RLD3_36B_QK2_P	DIFF_SSTL12
H29	RLD3_36B_QK2_N	DIFF_SSTL12
M31	RLD3_36B_QK3_P	DIFF_SSTL12
L31	RLD3_36B_QK3_N	DIFF_SSTL12
A26	RLD3_36B_QVLD0	SSTL12
G27	RLD3_36B_QVLD1	SSTL12
D25	RLD3_36B_A0	SSTL12
C24	RLD3_36B_A3	SSTL12

Table 1-5: **RLD3 Memory U141 36-bit I/F to FPGA U1 Banks 70 and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard
D24	RLD3_36B_A4	SSTL12
F23	RLD3_36B_A5	SSTL12
E23	RLD3_36B_A8	SSTL12
B22	RLD3_36B_A9	SSTL12
C23	RLD3_36B_A10	SSTL12
G21	RLD3_36B_A13	SSTL12
F24	RLD3_36B_A14	SSTL12
A23	RLD3_36B_A17	SSTL12
B23	RLD3_36B_A18	SSTL12
C25	RLD3_36B_BA0	SSTL12
E24	RLD3_36B_BA1	SSTL12
B25	RLD3_36B_BA2	SSTL12
C22	RLD3_36B_BA3	SSTL12
A25	RLD3_36B_WE_B	SSTL12
A24	RLD3_36B_REF_B	SSTL12
G25	RLD3_36B_CK_P	DIFF_SSTL12
F25	RLD3_36B_CK_N	DIFF_SSTL12
F21	RLD3_36B_RESET_B	SSTL12
E22	RLD3_36B_CS_B	SSTL12
H23	RLD3_36B_DK0_P	DIFF_SSTL12
G23	RLD3_36B_DK0_N	DIFF_SSTL12
H22	RLD3_36B_DK1_P	DIFF_SSTL12
G22	RLD3_36B_DK1_N	DIFF_SSTL12

The connections between RLD3 component memory U173 and XCVU190 bank 72 are listed in Table 1-6.

Table 1-6: **RLD3 Memory U173 18-bit I/F to FPGA U1 Bank 72**

FPGA (U1) Pin	Schematic Net Name	I/O Standard
K16	RLD3_18B_DQ0	SSTL12
L15	RLD3_18B_DQ1	SSTL12
L20	RLD3_18B_DQ2	SSTL12
L18	RLD3_18B_DQ3	SSTL12
J16	RLD3_18B_DQ4	SSTL12
L19	RLD3_18B_DQ5	SSTL12
K18	RLD3_18B_DQ6	SSTL12

Table 1-6: **RLD3 Memory U173 18-bit I/F to FPGA U1 Bank 72 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard
M20	RLD3_18B_DQ7	SSTL12
K19	RLD3_18B_DQ8	SSTL12
N19	RLD3_18B_DQ9	SSTL12
M16	RLD3_18B_DQ10	SSTL12
M17	RLD3_18B_DQ11	SSTL12
N20	RLD3_18B_DQ12	SSTL12
P16	RLD3_18B_DQ13	SSTL12
M15	RLD3_18B_DQ14	SSTL12
P17	RLD3_18B_DQ15	SSTL12
P20	RLD3_18B_DQ16	SSTL12
P19	RLD3_18B_DQ17	SSTL12
L16	RLD3_18B_DM0	SSTL12
N17	RLD3_18B_DM1	SSTL12
A20	RLD3_18B_A0	SSTL12
F20	RLD3_18B_A3	SSTL12
E18	RLD3_18B_A4	SSTL12
H18	RLD3_18B_A5	SSTL12
G18	RLD3_18B_A8	SSTL12
H19	RLD3_18B_A9	SSTL12
J19	RLD3_18B_A10	SSTL12
F18	RLD3_18B_A13	SSTL12
A19	RLD3_18B_A14	SSTL12
H20	RLD3_18B_A17	SSTL12
J20	RLD3_18B_A18	SSTL12
E19	RLD3_18B_BA0	SSTL12
A18	RLD3_18B_BA1	SSTL12
B20	RLD3_18B_BA2	SSTL12
G20	RLD3_18B_BA3	SSTL12
B18	RLD3_18B_WE_B	SSTL12
C20	RLD3_18B_REF_B	SSTL12
D20	RLD3_18B_CK_P	DIFF_SSTL12
D19	RLD3_18B_CK_N	DIFF_SSTL12
E21	RLD3_18B_RESET_B	SSTL12
F19	RLD3_18B_CS_B	SSTL12
B21	RLD3_18B_DK0_P	DIFF_SSTL12

Table 1-6: **RLD3 Memory U173 18-bit I/F to FPGA U1 Bank 72 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard
A21	RLD3_18B_DK0_N	DIFF_SSTL12
C19	RLD3_18B_DK1_P	DIFF_SSTL12
C18	RLD3_18B_DK1_N	DIFF_SSTL12
K17	RLD3_18B_QK0_P	DIFF_SSTL12
J17	RLD3_18B_QK0_N	DIFF_SSTL12
N18	RLD3_18B_QK1_P	DIFF_SSTL12
M18	RLD3_18B_QK1_N	DIFF_SSTL12
J15	RLD3_18B_QVLD0	SSTL12

The VCU110 RLD3 36-bit and 18-bit memory component interfaces adhere to the constraints guidelines documented in the RLD3 Design Guidelines section of *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150) [Ref 3] for Vivado Design Suite. The VCU110 RLD3 memory component interface is a 40Ω impedance implementation.

For more details about the Micron RLD3 component memory, see the Micron MT44K16M36RB-093E/ MT44K32M18RB-093E data sheet [Ref 21].

Dual Quad-SPI Flash Memory

[Figure 1-2, callout 6]

The dual 512 Mb Quad-SPI flash memories are located at U182 and U183 and provide 1 Gb of nonvolatile storage that can be used for configuration and data storage.

- Part number: MT25QU512ABA8E12-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 8 bits
- Data rate: various depending on Single/Dual/Quad mode

Note: For details on bank 0 pins, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

Figure 1-6 shows the connections of the linear dual Quad-SPI flash memory on the VCU110 evaluation board. For more details, see the Micron N25QU512ABA8E12-0SIT data sheet [Ref 21].

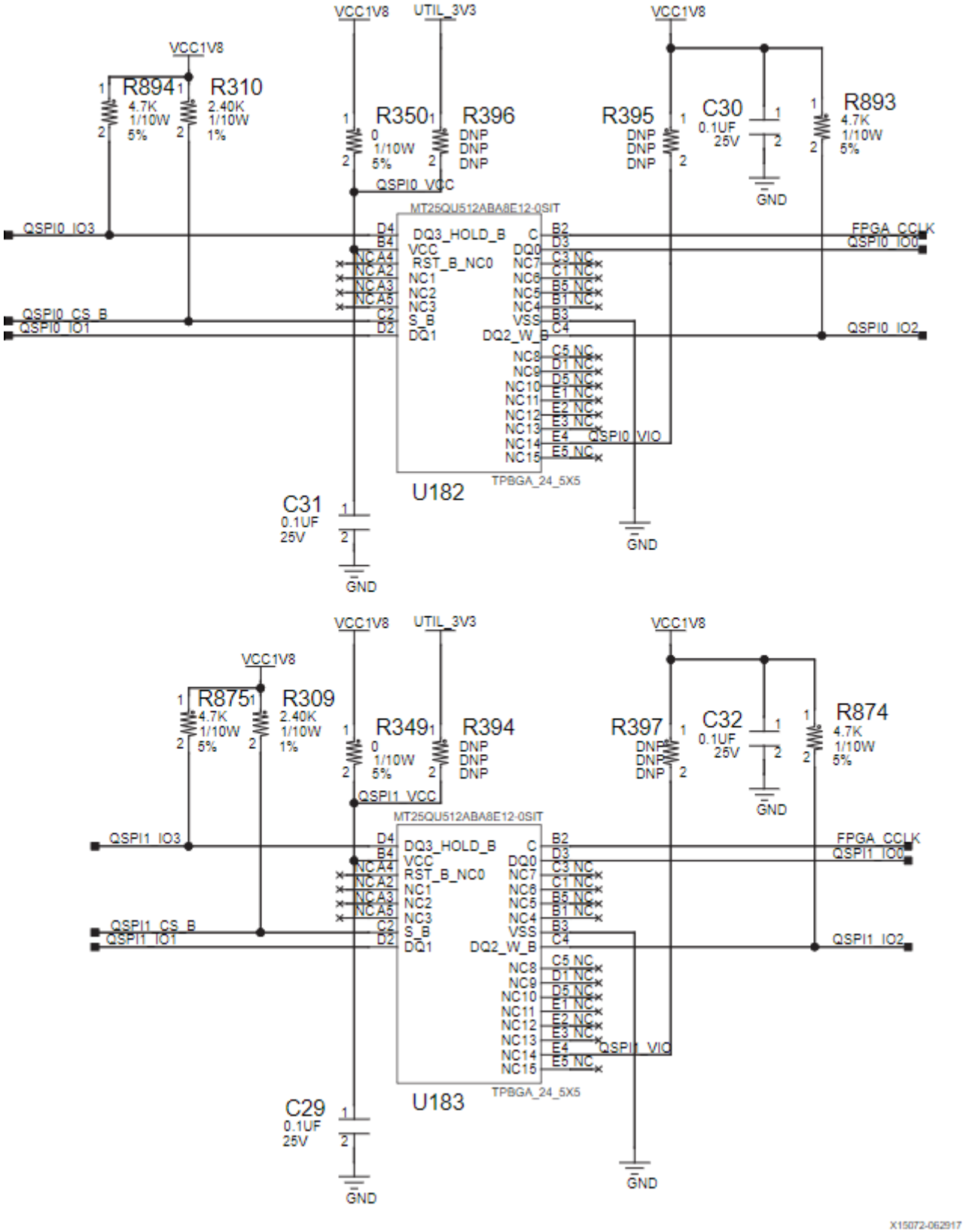

Figure 1-6: **Dual 512 Mb Quad-SPI Flash Memory**

The connections between the dual Quad SPI components U182, U183 and XCVU190 banks 0 and 65 are listed in Table 1-7.

Table 1-7: **Dual-QSPI Memory U182, U183 I/F to FPGA U1 Banks 0 and 65**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	QSPI Memory		
			Pin Number	Pin Name	Reference Designator
AM14	QSPI0_IO0	(1)	D3	DQ0	U182
AK14	QSPI0_IO1	(1)	D2	DQ1	U182
AF16	QSPI0_IO2	(1)	C4	DQ2_W_B	U182
AH14	QSPI0_IO3	(1)	D4	DQ3_HOLD_B	U182
AF14	QSPI0_CS_B	(1)	C2	S_B	U182
AB16	FPGA_CCLK	(1)	B2	C	U182
BE19	QSPI1_IO0	LVCMOS18	D3	DQ0	U183
BF19	QSPI1_IO1	LVCMOS18	D2	DQ1	U183
BD18	QSPI1_IO2	LVCMOS18	C4	DQ2_W_B	U183
BE18	QSPI1_IO3	LVCMOS18	D4	DQ3_HOLD_B	U183
AP20	QSPI1_CS_B	LVCMOS18	C2	S_B	U183
AB16	FPGA_CCLK	(1)	B2	C	U183

Notes:

1. Bank 0 V_{CCO} = 1.8V; bank 0 I/O standards are not specified.

Hybrid Memory Cube

[Figure 1-2, callout 7]

The HMC component memory system is comprised of one 16-lane 2 GB device (Micron MT43A4G40200NFA) located at U160. This memory system is connected to the XCVU190 MGTH banks 225-232 (8 MGTH Quads).

The connections between the HMC component U160 bank L0 and XCVU190 GTH Quads 229-232 are listed in Table 1-8. The nets with _C_P or _C_N in their net names are series capacitor coupled.

Table 1-8: **HMC Memory U160 L0 I/F to FPGA U1 GTH Quads 229-232**

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[(1)]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 229	MGTHTXP0_229	R7	HMC_L0TX_12_P	G18	L0RXP_0	HMC U160
	MGTHTXN0_229	R6	HMC_L0TX_12_N	G17	L0RXN_0	
	MGTHRXP0_229	R2	HMC_L0RX_12_C_P	E24	L0TXP_0	
	MGTHRXN0_229	R1	HMC_L0RX_12_C_N	E23	L0TXN_0	
	MGTHTXP1_229	P9	HMC_L0TX_9_P	F19	L0RXP_1	
	MGTHTXN1_229	P8	HMC_L0TX_9_N	F18	L0RXN_1	
	MGTHRXP1_229	P4	HMC_L0RX_9_C_P	F23	L0TXP_1	
	MGTHRXN1_229	P3	HMC_L0RX_9_C_N	F22	L0TXN_1	
	MGTHTXP2_229	N7	HMC_L0TX_13_P	A16	L0RXP_2	
	MGTHTXN2_229	N6	HMC_L0TX_13_N	A15	L0RXN_2	
	MGTHRXP2_229	N2	HMC_L0RX_13_C_P	D17	L0TXP_2	
	MGTHRXN2_229	N1	HMC_L0RX_13_C_N	D16	L0TXN_2	
	MGTHTXP3_229	M9	HMC_L0TX_8_P	A24	L0RXP_3	
	MGTHTXN3_229	M8	HMC_L0TX_8_N	A23	L0RXN_3	
	MGTHRXP3_229	M4	HMC_L0RX_8_C_P	C18	L0TXP_3	
	MGTHRXN3_229	M3	HMC_L0RX_8_C_N	C17	L0TXN_3	
	MGTREFCLK0P_229	U11	NA	NA	NA	NA
	MGTREFCLK0N_229	U10	NA	NA	NA	
	MGTREFCLK1P_229	T13	NA	NA	NA	
	MGTREFCLK1N_229	T12	NA	NA	NA	

Table 1-8: **HMC Memory U160 L0 I/F to FPGA U1 GTH Quads 229-232 *(Cont'd)***

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 230	MGTHTXP0_230	L7	HMC_L0TX_10_P	E20	L0RXP_4	HMC U160
	MGTHTXN0_230	L6	HMC_L0TX_10_N	E19	L0RXN_4	
	MGTHRXP0_230	L2	HMC_L0RX_10_C_P	D25	L0TXP_4	
	MGTHRXN0_230	L1	HMC_L0RX_10_C_N	D24	L0TXN_4	
	MGTHTXP1_230	K9	HMC_L0TX_14_P	D21	L0RXP_5	
	MGTHTXN1_230	K8	HMC_L0TX_14_N	D20	L0RXN_5	
	MGTHRXP1_230	K4	HMC_L0RX_14_C_P	B27	L0TXP_5	
	MGTHRXN1_230	K3	HMC_L0RX_14_C_N	B26	L0TXN_5	
	MGTHTXP2_230	J7	HMC_L0TX_0_P	C22	L0RXP_6	
	MGTHTXN2_230	J6	HMC_L0TX_0_N	C21	L0RXN_6	
	MGTHRXP2_230	J2	HMC_L0RX_0_C_P	A20	L0TXP_6	
	MGTHRXN2_230	J1	HMC_L0RX_0_C_N	A19	L0TXN_6	
	MGTHTXP3_230	H9	HMC_L0TX_1_P	B23	L0RXP_7	
	MGTHTXN3_230	H8	HMC_L0TX_1_N	B22	L0RXN_7	
	MGTHRXP3_230	H4	HMC_L0RX_1_C_P	B19	L0TXP_7	
	MGTHRXN3_230	H3	HMC_L0RX_1_C_N	B18	L0TXN_7	
	MGTREFCLK0P_230	R11	HMC_SI5328_OUT2_BUF1_C_P	35	CKOUT2_P	SI5328 U57
	MGTREFCLK0N_230	R10	HMC_SI5328_OUT2_BUF1_C_N	34	CKOUT2_N	
	MGTREFCLK1P_230	P13	NA	NA	NA	NA
	MGTREFCLK1N_230	P12	NA	NA	NA	

Table 1-8: **HMC Memory U160 L0 I/F to FPGA U1 GTH Quads 229-232 *(Cont'd)***

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 231	MGTHTXP0_231	G7	HMC_L0TX_4_P	L30	L0RXP_8	HMC U160
	MGTHTXN0_231	G6	HMC_L0TX_4_N	L29	L0RXN_8	
	MGTHRXP0_231	G2	HMC_L0RX_4_C_P	K27	L0TXP_8	
	MGTHRXN0_231	G1	HMC_L0RX_4_C_N	K26	L0TXN_8	
	MGTHTXP1_231	F9	HMC_L0TX_11_P	M28	L0RXP_9	
	MGTHTXN1_231	F8	HMC_L0TX_11_N	M27	L0RXN_9	
	MGTHRXP1_231	F4	HMC_L0RX_11_C_P	L26	L0TXP_9	
	MGTHRXN1_231	F3	HMC_L0RX_11_C_N	L25	L0TXN_9	
	MGTHTXP2_231	G11	HMC_L0TX_6_P	C30	L0RXP_10	
	MGTHTXN2_231	G10	HMC_L0TX_6_N	C29	L0RXN_10	
	MGTHRXP2_231	G16	HMC_L0RX_6_C_P	G22	L0TXP_10	
	MGTHRXN2_231	G15	HMC_L0RX_6_C_N	G21	L0TXN_10	
	MGTHTXP3_231	F13	HMC_L0TX_2_P	D29	L0RXP_11	
	MGTHTXN3_231	F12	HMC_L0TX_2_N	D28	L0RXN_11	
	MGTHRXP3_231	E16	HMC_L0RX_2_C_P	C26	L0TXP_11	
	MGTHRXN3_231	E15	HMC_L0RX_2_C_N	C25	L0TXN_11	
	MGTREFCLK0P_231	N11	NA	NA	NA	NA
	MGTREFCLK0N_231	N10	NA	NA	NA	
	MGTREFCLK1P_231	M13	NA	NA	NA	
	MGTREFCLK1N_231	M12	NA	NA	NA	

Table 1-8: **HMC Memory U160 L0 I/F to FPGA U1 GTH Quads 229-232 *(Cont'd)***

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 232	MGTHTXP0_232	E7	HMC_L0TX_3_P	H25	L0RXP_12	HMC U160
	MGTHTXN0_232	E6	HMC_L0TX_3_N	H24	L0RXN_12	
	MGTHRXP0_232	E2	HMC_L0RX_3_C_P	J28	L0TXP_12	
	MGTHRXN0_232	E1	HMC_L0RX_3_C_N	J27	L0TXN_12	
	MGTHTXP1_232	E11	HMC_L0TX_15_P	G26	L0RXP_13	
	MGTHTXN1_232	E10	HMC_L0TX_15_N	G25	L0RXN_13	
	MGTHRXP1_232	D4	HMC_L0RX_15_C_P	H29	L0TXP_13	
	MGTHRXN1_232	D3	HMC_L0RX_15_C_N	H28	L0TXN_13	
	MGTHTXP2_232	C7	HMC_L0TX_5_P	F27	L0RXP_14	
	MGTHTXN2_232	C6	HMC_L0TX_5_N	F26	L0RXN_14	
	MGTHRXP2_232	C2	HMC_L0RX_5_C_P	G30	L0TXP_14	
	MGTHRXN2_232	C1	HMC_L0RX_5_C_N	G29	L0TXN_14	
	MGTHTXP3_232	A7	HMC_L0TX_7_P	E28	L0RXP_15	
	MGTHTXN3_232	A6	HMC_L0TX_7_N	E27	L0RXN_15	
	MGTHRXP3_232	B4	HMC_L0RX_7_C_P	A28	L0TXP_15	
	MGTHRXN3_232	B3	HMC_L0RX_7_C_N	A27	L0TXN_15	
	MGTREFCLK0P_232	L11	NA	NA	NA	NA
	MGTREFCLK0N_232	L10	NA	NA	NA	
	MGTREFCLK1P_232	K13	NA	NA	NA	
	MGTREFCLK1N_232	K12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.

The connections between the HMC component U160 bank L1 and XCVU190 GTH Quads (225-228) are listed in Table 1-9. The nets with _C_P or _C_N in their net names are series capacitor coupled.

Table 1-9: **HMC Memory U160 L1 I/F to FPGA U1 GTH Quads 225-228**

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 225	MGTHTXP0_225	AL7	HMC_L1TX_0_P	AD18	L1RXP_0	HMC U160
	MGTHTXN0_225	AL6	HMC_L1TX_0_N	AD17	L1RXN_0	
	MGTHRXP0_225	AL2	HMC_L1RX_0_C_P	AF24	L1TXP_0	
	MGTHRXN0_225	AL1	HMC_L1RX_0_C_N	AF23	L1TXN_0	
	MGTHTXP1_225	AK9	HMC_L1TX_2_P	AE19	L1RXP_1	
	MGTHTXN1_225	AK8	HMC_L1TX_2_N	AE18	L1RXN_1	
	MGTHRXP1_225	AK4	HMC_L1RX_2_C_P	AE23	L1TXP_1	
	MGTHRXN1_225	AK3	HMC_L1RX_2_C_N	AE22	L1TXN_1	
	MGTHTXP2_225	AJ7	HMC_L1TX_1_P	AK16	L1RXP_2	
	MGTHTXN2_225	AJ6	HMC_L1TX_1_N	AK15	L1RXN_2	
	MGTHRXP2_225	AJ2	HMC_L1RX_1_C_P	AG17	L1TXP_2	
	MGTHRXN2_225	AJ1	HMC_L1RX_1_C_N	AG16	L1TXN_2	
	MGTHTXP3_225	AH9	HMC_L1TX_6_P	AK24	L1RXP_3	
	MGTHTXN3_225	AH8	HMC_L1TX_6_N	AK23	L1RXN_3	
	MGTHRXP3_225	AH4	HMC_L1RX_6_C_P	AH18	L1TXP_3	
	MGTHRXN3_225	AH3	HMC_L1RX_6_C_N	AH17	L1TXN_3	
	MGTREFCLK0P_225	AE11	NA	NA	NA	NA
	MGTREFCLK0N_225	AE10	NA	NA	NA	
	MGTREFCLK1P_225	AD13	NA	NA	NA	
	MGTREFCLK1N_225	AD12	NA	NA	NA	

Table 1-9: **HMC Memory U160 L1 I/F to FPGA U1 GTH Quads 225-228 *(Cont'd)***

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 226	MGTHTXP0_226	AG7	HMC_L1TX_4_P	AG29	L1RXP_11	HMC U160
	MGTHTXN0_226	AG6	HMC_L1TX_4_N	AG28	L1RXN_11	
	MGTHRXP0_226	AG2	HMC_L1RX_4_C_P	AH26	L1TXP_11	
	MGTHRXN0_226	AG1	HMC_L1RX_4_C_N	AH25	L1TXN_11	
	MGTHTXP1_226	AF9	HMC_L1TX_3_P	AH30	L1RXP_10	
	MGTHTXN1_226	AF8	HMC_L1TX_3_N	AH29	L1RXN_10	
	MGTHRXP1_226	AF4	HMC_L1RX_3_C_P	AD22	L1TXP_10	
	MGTHRXN1_226	AF3	HMC_L1RX_3_C_N	AD21	L1TXN_10	
	MGTHTXP2_226	AE7	HMC_L1TX_7_P	W28	L1RXP_9	
	MGTHTXN2_226	AE6	HMC_L1TX_7_N	W27	L1RXN_9	
	MGTHRXP2_226	AE2	HMC_L1RX_7_C_P	Y26	L1TXP_9	
	MGTHRXN2_226	AE1	HMC_L1RX_7_C_N	Y25	L1TXN_9	
	MGTHTXP3_226	AD9	HMC_L1TX_5_P	Y30	L1RXP_8	
	MGTHTXN3_226	AD8	HMC_L1TX_5_N	Y29	L1RXN_8	
	MGTHRXP3_226	AD4	HMC_L1RX_5_C_P	AA27	L1TXP_8	
	MGTHRXN3_226	AD3	HMC_L1RX_5_C_N	AA28	L1TXN_8	
	MGTREFCLK0P_226	AC11	HMC_SI5328_OUT2_BUF2_C_P	35	CKOUT2_P	SI5328 U57
	MGTREFCLK0N_226	AC10	HMC_SI5328_OUT2_BUF2_C_N	34	CKOUT2_N	
	MGTREFCLK1P_226	AB13	NA	NA	NA	NA
	MGTREFCLK1N_226	AB12	NA	NA	NA	

Table 1-9: **HMC Memory U160 L1 I/F to FPGA U1 GTH Quads 225-228 *(Cont'd)***

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 227	MGTHTXP0_227	AC7	HMC_L1TX_11_P	AJ23	L1RXP_7	HMC U160
	MGTHTXN0_227	AC6	HMC_L1TX_11_N	AJ22	L1RXN_7	
	MGTHRXP0_227	AC2	HMC_L1RX_11_C_P	AJ19	L1TXP_7	
	MGTHRXN0_227	AC1	HMC_L1RX_11_C_N	AJ18	L1TXN_7	
	MGTHTXP1_227	AB9	HMC_L1TX_14_P	AH22	L1RXP_6	
	MGTHTXN1_227	AB8	HMC_L1TX_14_N	AH21	L1RXN_6	
	MGTHRXP1_227	AB4	HMC_L1RX_14_C_P	AK20	L1TXP_6	
	MGTHRXN1_227	AB3	HMC_L1RX_14_C_N	AK19	L1TXN_6	
	MGTHTXP2_227	AA7	HMC_L1TX_15_P	AG21	L1RXP_5	
	MGTHTXN2_227	AA6	HMC_L1TX_15_N	AG20	L1RXN_5	
	MGTHRXP2_227	AA2	HMC_L1RX_15_C_P	AJ27	L1TXP_5	
	MGTHRXN2_227	AA1	HMC_L1RX_15_C_N	AJ26	L1TXN_5	
	MGTHTXP3_227	Y9	HMC_L1TX_13_P	AF20	L1RXP_4	
	MGTHTXN3_227	Y8	HMC_L1TX_13_N	AF19	L1RXN_4	
	MGTHRXP3_227	Y4	HMC_L1RX_13_C_P	AG25	L1TXP_4	
	MGTHRXN3_227	Y3	HMC_L1RX_13_C_N	AG24	L1TXN_4	
	MGTREFCLK0P_227	AA11	NA	NA	NA	NA
	MGTREFCLK0N_227	AA10	NA	NA	NA	
	MGTREFCLK1P_227	Y13	NA	NA	NA	
	MGTREFCLK1N_227	Y12	NA	NA	NA	

Table 1-9: **HMC Memory U160 L1 I/F to FPGA U1 GTH Quads 225-228 *(Cont'd)***

MGT Bank	FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
GTH Quad 228	MGTHTXP0_228	W7	HMC_L1TX_12_P	AK24	L1RXP_3	HMC U160
	MGTHTXN0_228	W6	HMC_L1TX_12_N	AK23	L1RXN_3	
	MGTHRXP0_228	W2	HMC_L1RX_12_C_P	AH18	L1TXP_3	
	MGTHRXN0_228	W1	HMC_L1RX_12_C_N	AH17	L1TXN_3	
	MGTHTXP1_228	V9	HMC_L1TX_10_P	AK16	L1RXP_2	
	MGTHTXN1_228	V8	HMC_L1TX_10_N	AK15	L1RXN_2	
	MGTHRXP1_228	V4	HMC_L1RX_10_C_P	AG17	L1TXP_2	
	MGTHRXN1_228	V3	HMC_L1RX_10_C_N	AG16	L1TXN_2	
	MGTHTXP2_228	U7	HMC_L1TX_9_P	AE19	L1RXP_1	
	MGTHTXN2_228	U6	HMC_L1TX_9_N	AE18	L1RXN_1	
	MGTHRXP2_228	U2	HMC_L1RX_9_C_P	AE23	L1TXP_1	
	MGTHRXN2_228	U1	HMC_L1RX_9_C_N	AE22	L1TXN_1	
	MGTHTXP3_228	T9	HMC_L1TX_8_P	AD18	L1RXP_0	
	MGTHTXN3_228	T8	HMC_L1TX_8_N	AD17	L1RXN_0	
	MGTHRXP3_228	T4	HMC_L1RX_8_C_P	AF24	L1TXP_0	
	MGTHRXN3_228	T3	HMC_L1RX_8_C_N	AF23	L1TXN_0	
	MGTREFCLK0P_228	W11	NA	NA	NA	NA
	MGTREFCLK0N_228	W10	NA	NA	NA	
	MGTREFCLK1P_228	V13	NA	NA	NA	
	MGTREFCLK1N_228	V12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.

The HMC component U160 control bank connections are listed in Table 1-10.

Table 1-10: **HMC Memory U160 Control I/F Connections**

HMC U160 Pin Number	HMC U160 Pin Name	Schematic Net Name[1]	I/O Standard	Connected Pin Number	Connected Device
U30	P_RST_N	HMC_P_RST_B	LVCMOS15	AW28	FPGA U1
N1	REFCLK_BOOT_0	HMC_REFCLK_BOOT_0	LVCMOS15	BA26	
U29	REFCLK_BOOT_1	HMC_REFCLK_BOOT_1	LVCMOS15	BB26	
V6	REFCLKSEL	HMC_REFCLK_SEL	LVCMOS15	AV30	
U5	FERR_N	HMC_FERR_B	LVCMOS15	AW30	
P29	L1RXPS	HMC_L1RXPS	LVCMOS15	BB27	
V24	L1TXPS	HMC_L1TXPS	LVCMOS15	AY29	
U28	L0RXPS	HMC_L0RXPS	LVCMOS15	AY30	
N24	L0TXPS	HMC_L0TXPS	LVCMOS15	AW27	
R30	REFCLKN	HMC_SI5328_OUT1_C_N[1]	NA	28	SI5328 U57
T30	REFCLKP	HMC_SI5328_OUT1_C_P[1]	NA	29	
R28	SCL	IIC_SCL_HMC_LS[2]	NA	16	IIC MUX U28
T24	SDA	IIC_SDA_HMC_LS[2]	NA	15	
T5	TCK	HMC_TCK	NA	5	JTAG connector J120
P7	TDI	HMC_TDI	NA	3	
T1	TDO	HMC_TDO	NA	2	
R5	TMS	HMC_TMS	NA	4	
R7	TRST_N	HMC_TRST_B	NA	6	

Notes:
1. Series capacitor coupled.
2. IIC is level shifted through U159.

For more details about HMC, see the Micron MT43A4G40200NFA data sheet [Ref 21].

Micro-SD Card Interface

[Figure 1-2, callout 8]

The VCU110 board includes a secure digital input/output (SDIO) interface to provide user access to general purpose nonvolatile micro-SD memory cards for configuration. The micro-SD card slot is designed to support 50 MHz high speed micro-SD cards. The SDIO signals are connected to U111 XC7Z010 Zynq SoC system controller bank 500, which has its V_{CCO} set to SYS_1V8 1.8V. A MAX13035E level-shifter (U154) is used between the XC7Z010 System Controller (U111) and the micro-SD card connector (J83).

USB JTAG Interface

[Figure 1-2, callout 9]

JTAG configuration is provided through a Digilent onboard USB-to-JTAG configuration logic module (U115) where a host computer accesses the VCU110 board JTAG chain through a type-A (host side) to micro-B (VCU110 board side) USB cable.

A 2 mm JTAG header (J3) is also provided in parallel for access by Xilinx download cables such as the Platform Cable USB II and the Parallel Cable IV. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pins M[2:0], wired to SW16 positions [1:3].

The JTAG chain of the VCU110 board is illustrated in Figure 1-7.

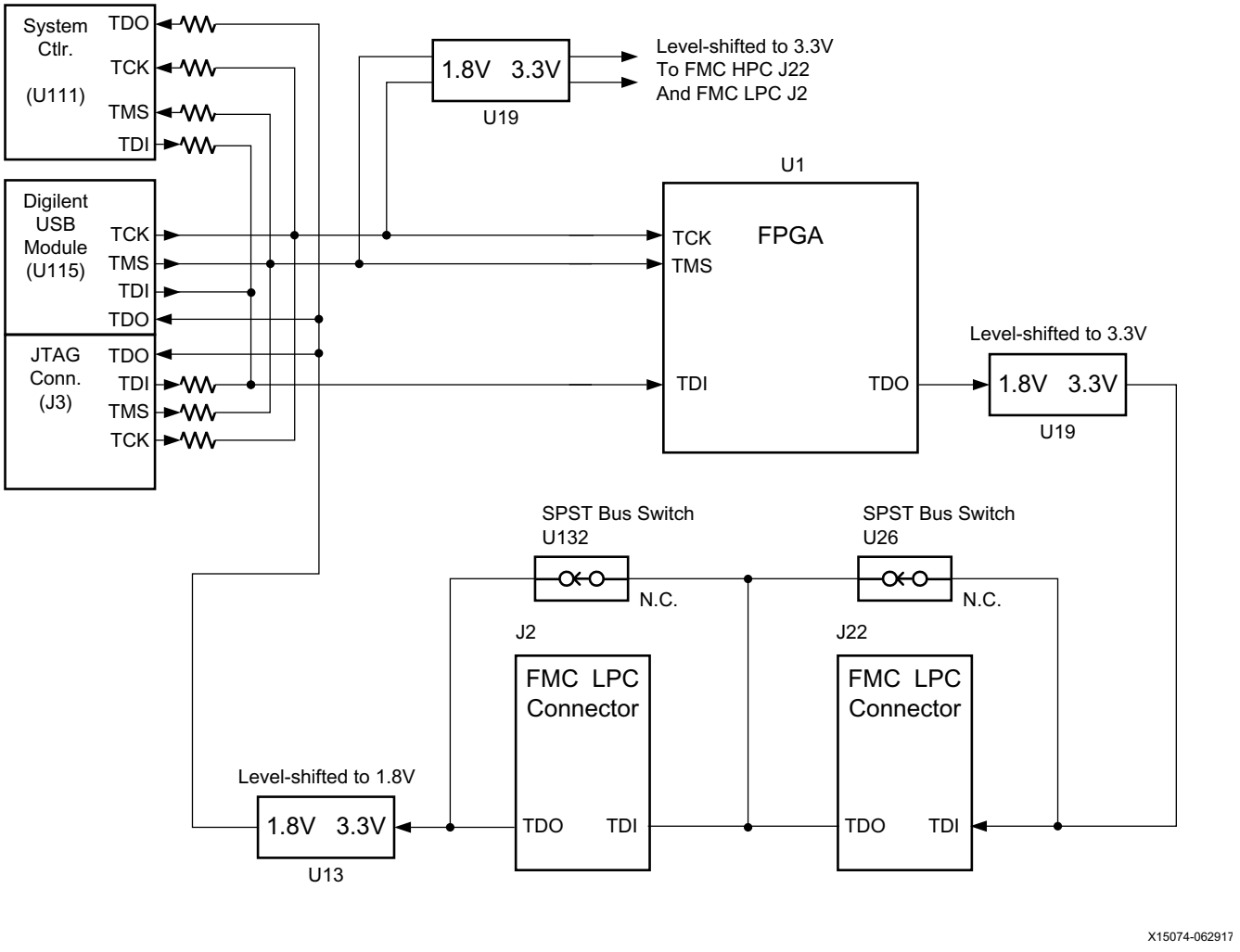

Figure 1-7: **JTAG Chain Block Diagram**

For more details about the Digilent USB JTAG module, see [Ref 24].

JTAG Chain FMC Connector Bypass

When an FMC mezzanine card is attached to the VCU110 board it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U26 (HPC0) and U132 (HPC1). The SPST switches are in a normally closed state and transition to an open state when an FMC mezzanine card is attached.

- Switch U26 adds an attached FMC HPC0 J22 mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC0_PRSNT_M2C_B signal.
- Switch U132 adds an attached FMC HPC1 J2 mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC1_PRSNT_M2C_B signal.

The attached FMC card must implement a TDI-to-TDO connection through a device or bypass jumper to ensure that the JTAG chain connects to the FPGA U1.

The JTAG connectivity on the VCU110 board allows a host computer to download bitstreams to the FPGA using Xilinx configuration software. In addition, the JTAG connector allows debug tools such as the Vivado serial I/O analyzer or a software debugger to access the FPGA. The Xilinx configuration software tool can also program the dual Quad SPI Flash memory.

Clock Generation

The VCU110 evaluation board provides fourteen clock sources to the FPGA and eleven to other board components (25 total), as listed in Table 1-11.

Table 1-11: **VCU110 Board Clock Sources**

Clock Name	Clock Reference Designator	Description
System clock 300 MHz	U122	Silicon Labs Si5335A LVDS any frequency Quad clock generator CLK0. (SYSCLK_300_P/N)
System clock 125 MHz	U122	Silicon Labs Si5335A LVDS any frequency Quad clock generator CLK1. (CLK_125MHZ_P/N)
EMC clock 90 MHz	U122	Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency Quad clock generator CLK2A. (FPGA_EMCCLK)
System controller U111 clock 33.333 MHz	U122	Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency Quad clock generator CLK3A. (SYSCTLR_CLK)
User clock 10 MHz - 810 MHz	U32	Silicon Labs Si570 LVDS I2C programmable oscillator, 156.250 MHz default. U32 (USER_SI570_CLOCK_P/N)
Jitter-attenuating clock multiplier	U57	Silicon Labs Si5328C LVDS precision clock multiplier CKOUT1 (HMC_SI5328_OUT1_P /N)
Jitter-attenuating clock multiplier	U57/U165	Silicon Labs Si5328C LVDS precision clock multiplier/jitter-attenuator CKOUT2 drives U165 Quad clock buffer (two buffered clocks HMC_SI5328_OUT2_BUF[1:2]_C_P /N)

Table 1-11: **VCU110 Board Clock Sources *(Cont'd)***

Clock Name	Clock Reference Designator	Description
Jitter-attenuating clock multiplier	U179/U180	Silicon Labs Si5328C LVDS precision clock multiplier/jitter-attenuator CKOUT1 drives U180 Quad clock buffer (four buffered clocks CFP4_SI5328_OUT1_BUF[1:4]_C_P/N)
Jitter-attenuating clock multiplier	U181/U184	Silicon Labs Si5328C LVDS precision clock multiplier/Jitter-attenuator CKOUT1 drives U184 Quad clock buffer (two buffered clocks EXAMAX_SI5328_OUT1_BUF[1:2]_C_P/N)
Jitter-attenuating clock multiplier	U181/U196	Silicon Labs Si5328C LVDS precision clock multiplier/Jitter-attenuator CKOUT2 drives U196 hex clock buffer (five buffered clocks ILKN_SI5328_OUT2_BUF[1:5]_C_P/N)
BULLSEYE1 connector	J87	Two external input clocks through BULLSEYE1 connector J87 (BULLSEYE1_GTY_REFCLK[0:1]_P/N)
BULLSEYE2 connector	J122	Two external input clocks through BULLSEYE2 connector J122 (BULLSEYE2_GTY_REFCLK[0:1]_P/N)
PCIe cable	J136	Two external input clocks through PCIe cable J136 (PCIE_CABLE_CLK_C_P/N)
USER_SMA_CLOCK	J34(P)/J35(N)	Two SMA input connectors J34/J35 (USER_SMA_CLOCK_P/N)

Table 1-12 lists the VCU110 clock sources connections.

Table 1-12: **VCU110 Clock Sources to XCVU190 FPGA U1 Connections**

Clock Source Reference Designator and Pin	Schematic Net Name	I/O Standard	Connected Pin	Connection or FPGA (U1) Bank
U122.22	SYSCLK_300_P	LVDS	J24	71
U122.21	SYSCLK_300_N	LVDS	H24	
U122.18	CLK_125MHZ_P	LVDS	AV20	65
U122.17	CLK_125MHZ_N	LVDS	AW20	
U122.14	FPGA_EMCCLK(1)	LVCMOS18	BE20	65
U122.10	SYSCTLR_CLK(1)	LVCMOS18	U111.C7	500
U32.4	USER_SI570_CLOCK_P	LVDS	AY20	65
U32.5	USER_SI570_CLOCK_N	LVDS	BA20	
U165.9	HMC_SI5328_OUT2_BUF1_C_P(2)	(3)	R11	GTH 230 REFCLK0
U165.10	HMC_SI5328_OUT2_BUF1_C_N(2)	(3)	R10	
U165.11	HMC_SI5328_OUT2_BUF2_C_P(2)	(3)	AC11	GTH 226 REFCLK0
U165.12	HMC_SI5328_OUT2_BUF2_C_N(2)	(3)	AC10	
U180.9	CFP4_SI5328_OUT1_BUF1_C_P(2)	(3)	AJ36	GTY 122 REFCLK0
U180.10	CFP4_SI5328_OUT1_BUF1_C_N(2)	(3)	AJ37	

Table 1-12: **VCU110 Clock Sources to XCVU190 FPGA U1 Connections *(Cont'd)***

Clock Source Reference Designator and Pin	Schematic Net Name	I/O Standard	Connected Pin	Connection or FPGA (U1) Bank
U180.11	CFP4_SI5328_OUT1_BUF2_C_P[2]	[3]	AE36	GTY 125 REFCLK0
U180.12	CFP4_SI5328_OUT1_BUF2_C_N[2]	[3]	AE37	
U180.13	CFP4_SI5328_OUT1_BUF3_C_P[2]	[3]	AA36	GTY127 REFCLK0
U180.14	CFP4_SI5328_OUT1_BUF3_C_N[2]	[3]	AA37	
U180.15	CFP4_SI5328_OUT1_BUF4_C_P[2]	[3]	W36	GTY128 REFCLK0
U180.16	CFP4_SI5328_OUT1_BUF4_C_N[2]	[3]	W37	
U184.9	EXAMAX_SI5328_OUT1_BUF1_C_P[2]	[3]	AN36	GTY 120 REFCLK0
U184.10	EXAMAX_SI5328_OUT1_BUF1_C_N[2]	[3]	AN37	
U184.11	EXAMAX_SI5328_OUT1_BUF2_C_P[2]	[3]	AL36	GTY 121 REFCLK0
U184.12	EXAMAX_SI5328_OUT1_BUF2_C_N[2]	[3]	AL37	
U196.5	ILKN_SI5328_OUT2_BUF1_C_P[2]	[3]	U36	GTY 129 REFCLK0
U196.4	ILKN_SI5328_OUT2_BUF1_C_N[2]	[3]	U37	
U196.32	ILKN_SI5328_OUT2_BUF2_C_P[2]	[3]	R36	GTY 130 REFCLK0
U196.31	ILKN_SI5328_OUT2_BUF2_C_N[2]	[3]	R37	
U196.30	ILKN_SI5328_OUT2_BUF3_C_P[2]	[3]	N36	GTY 131 REFCLK0
U196.29	ILKN_SI5328_OUT2_BUF3_C_N[2]	[3]	N37	
U196.28	ILKN_SI5328_OUT2_BUF4_C_P[2]	[3]	L36	GTY 132 REFCLK0
U196.27	ILKN_SI5328_OUT2_BUF4_C_N[2]	[3]	L37	
U196.26	ILKN_SI5328_OUT2_BUF5_C_P[2]	[3]	J36	GTY 133 REFCLK0
U196.25	ILKN_SI5328_OUT2_BUF5_C_N[2]	[3]	J37	
J87.19	BULLSEYE1_GTY_REFCLK0_C_P[2]	[3]	AC36	GTY 126 REFCLK0
J87.20	BULLSEYE1_GTY_REFCLK0_C_N[2]	[3]	AC37	
J87.1	BULLSEYE1_GTY_REFCLK1_C_P[2]	[3]	AB34	GTY 126 REFCLK1
J87.2	BULLSEYE1_GTY_REFCLK1_C_N[2]	[3]	AB35	
J122.19	BULLSEYE2_GTY_REFCLK0_C_P[2]	[3]	AG36	GTY 124 REFCLK0
J122.20	BULLSEYE2_GTY_REFCLK0_C_N[2]	[3]	AG37	
J122.1	BULLSEYE2_GTY_REFCLK1_C_P[2]	[3]	AF34	GTY 124 REFCLK1
J122.2	BULLSEYE2_GTY_REFCLK1_C_N[2]	[3]	AF35	
J136.A14	PCIE_CABLE_CLK_C_P[2]	[3]	J11	GTH 233 REFCLK0
J136.A15	PCIE_CABLE_CLK_C_N[2]	[3]	J10	

Table 1-12: **VCU110 Clock Sources to XCVU190 FPGA U1 Connections *(Cont'd)***

Clock Source Reference Designator and Pin	Schematic Net Name	I/O Standard	Connected Pin	Connection or FPGA (U1) Bank
J34.1	USER_SMA_CLOCK_P	LVDS	AY27	67
J35.1	USER_SMA_CLOCK_N	LVDS	AY28	

Notes:

1. Series resistor coupled.
2. Series capacitor coupled.
3. MGT connections I/O standard not applicable.

For more details on the Silicon Labs SI5335A, SI570, SI53340 and SI5328C devices, see [Ref 25].

UltraScale FPGA clocking information may be found in the *UltraScale Architecture Clocking Resources User Guide* (UG572) [Ref 4].

System Clock

[Figure 1-2, callout 10]

The system clock source is a Silicon Labs SI5335A Quad clock generator/buffer (U122). The system clock (SYSCLK_300_P/N) is a LVDS 300 MHz clock sourced from the CLK0A output pair of U122. The SYSCLK_300_P/N pair is connected to XCVU190 FPGA U1 bank 71 global clock (GC) pins J24 and H24, respectively.

- Clock generator: Silicon Labs SI5335A-B03426-GM (CLK0A 300 MHz)
- Low phase jitter of 0.7 ps RMS
- LVDS differential output

The 300 MHz system clock circuit is shown in Figure 1-8.

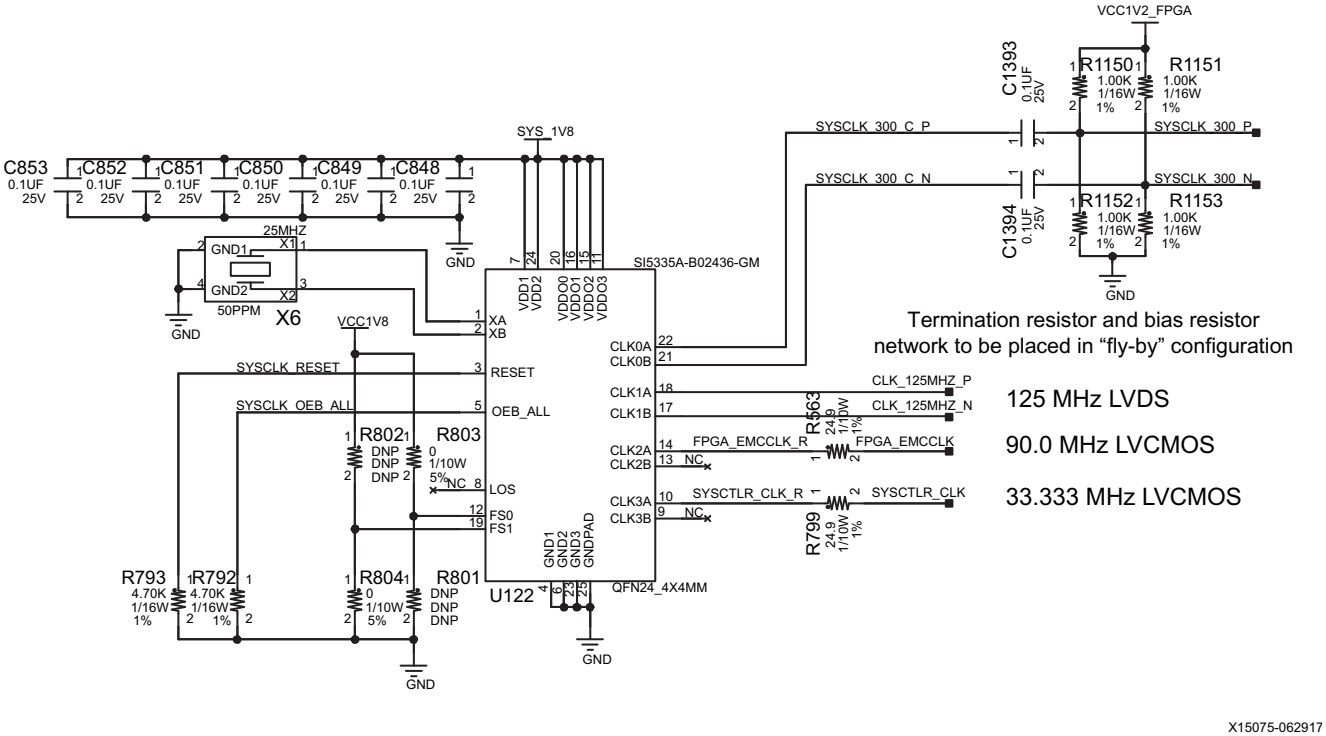

Figure 1-8: **300 MHz System Clock**

Three additional clocks are sourced from the U122 Quad clock generator:

- 125 MHz LVDS signal pair CLK_125MHZ_P and CLK_125MHZ_N, connected to XCVU190 FPGA U1 bank 65 pins AV20 and AW20, respectively.
- 90.0 MHz single-ended 1.8V LVCMOS, series resistor coupled FPGA_EMCCLK, connected to XCVU190 FPGA U1 bank 65 dedicated EMCCLK input pin BE20.
- 33.3333 MHz single-ended 1.8V LVCMOS, series resistor coupled SYSCTLR_CLK, connected to system controller XC7Z010 Zynq SoC U111 bank 500 dedicated PS_CLK input pin C7.

Programmable User Clock

[Figure 1-2, callout 11]

The VCU110 evaluation board has a SI570 programmable low-jitter LVDS differential oscillator (U32). The U32 output drives clock pair USER_SI570_CLOCK_P and USER_SI570_CLOCK_N, connected to XCVU190 FPGA U1 HR bank 65 GC pins AY20 and BA20, respectively.

On power-up, the U32 SI570 user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz

through an I2C interface. Power cycling the VCU110 evaluation board resets the user clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency jitter: 50 ppm
- LVDS differential output

The programmable clock circuit is shown in Figure 1-9.

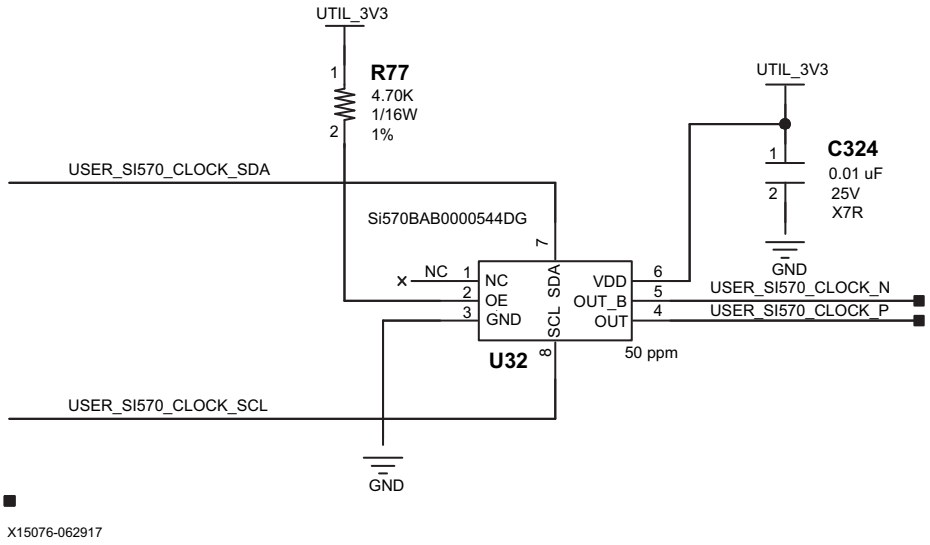

Figure 1-9: **User Clock**

Jitter-Attenuating Clock Multipliers

[Figure 1-2, callout 12, 13 and 14]

The VCU110 board hosts three Silicon Labs SI5328C jitter-attenuating clock multipliers (U57, U181, and U179) on the back of the board.

The SI5328C U57 HMC clock multiplier is used to generate the multiple clock frequencies required to drive the U160 HMC device and FPGA MGTH interface.

The U57 jitter attenuated clock multiplier circuit is shown in Figure 1-10.

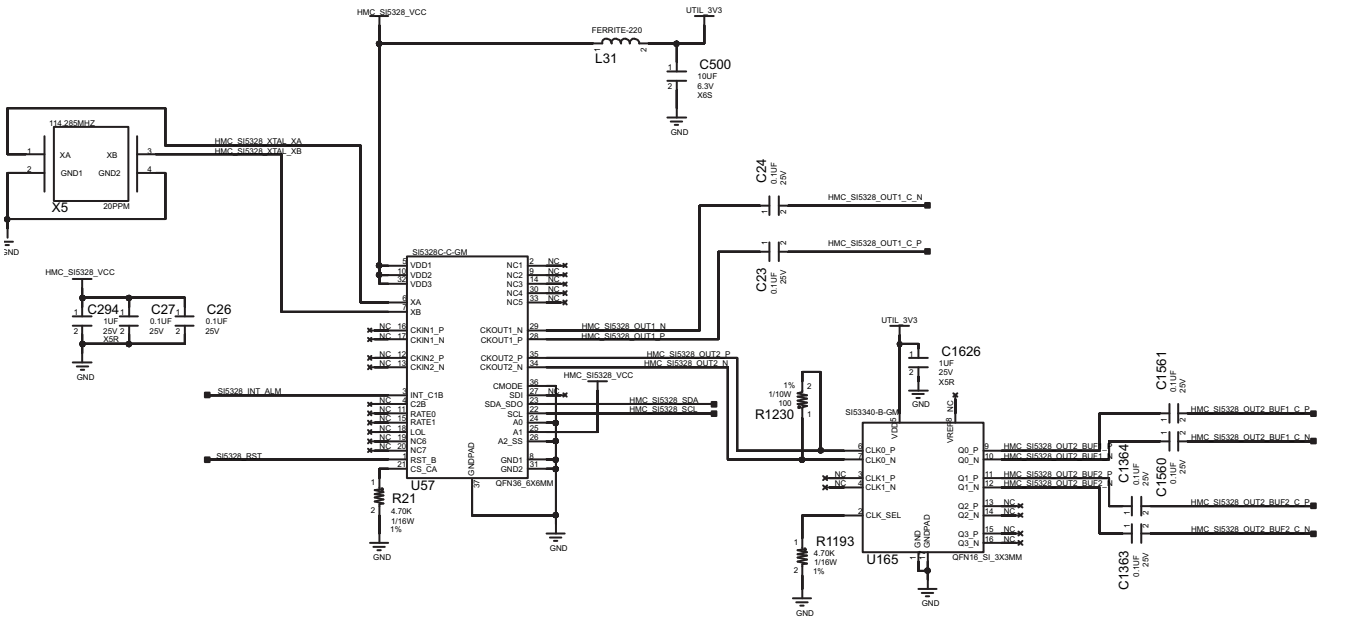

Figure 1-10: **HMC Jitter-Attenuating Clock Multiplier**

The VCU110 board second Silicon Labs SI5328C jitter attenuator U179 is on the back side of the board. FPGA U1 user logic can implement a clock recovery circuit and then output this clock to a differential I/O pair on I/O bank 128 (CFP4_REC_CLOCK2_C_P, U1 pin V34 and CFP4_REC_CLOCK2_C_N, U1 pin V35) for jitter attenuation. The jitter attenuated clock (CFP4_SI5328_OUT1_P (U179 pin 28) and CFP4_SI5328_OUT1_N (U179 pin 29)) are then routed as a reference clock to GTY Quads 125, 127, 128 and 131 REFCLK0 clock inputs as detailed in the GTY Transceivers section.

The primary purpose of this clock is to support CPRI/OBSAI applications that perform clock recovery from a user-supplied CFP4 module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTY transceiver.

The U179/U180 jitter attenuated clock multiplier circuit is shown in Figure 1-11.

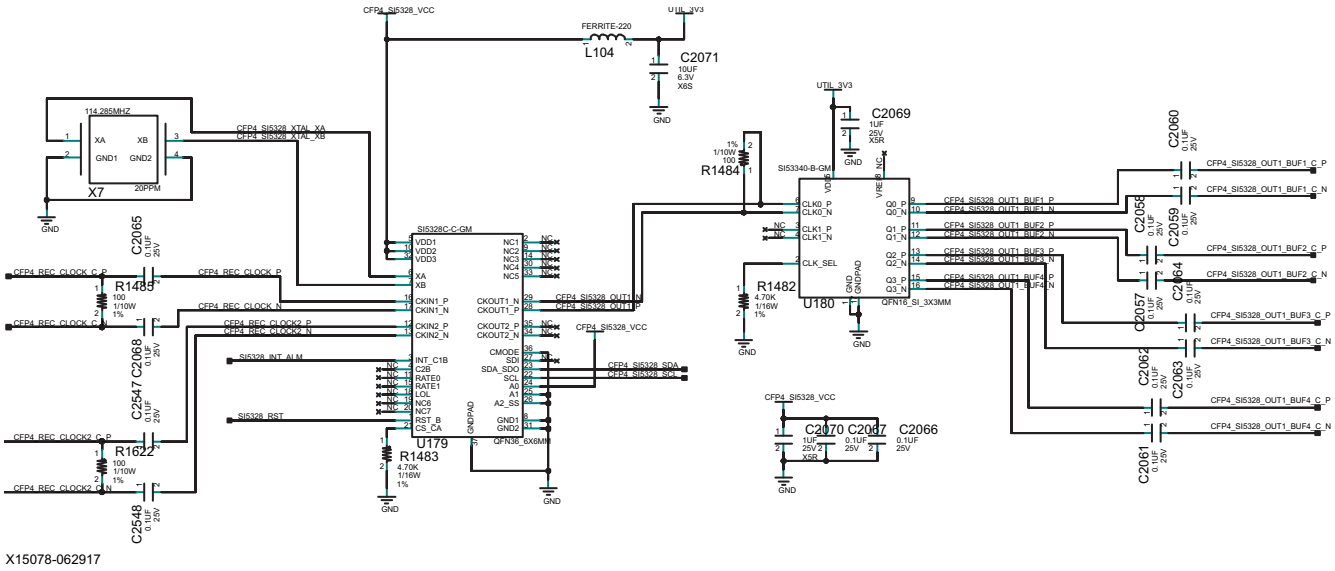

Figure 1-11: **CFP4 Interface Jitter-Attenuating Clock Multiplier**

For more details on the Silicon Labs SI5335A, SI570, SI53340 and SI5328C devices, see [Ref 25].

The SI5328C U179 HMC clock multiplier is used to generate the multiple clock frequencies required to drive the U160 HMC device and FPGA MGTH interface.

The third SI5328 U181 jitter-attenuated clock multiplier circuit is shown in Figure 1-12.

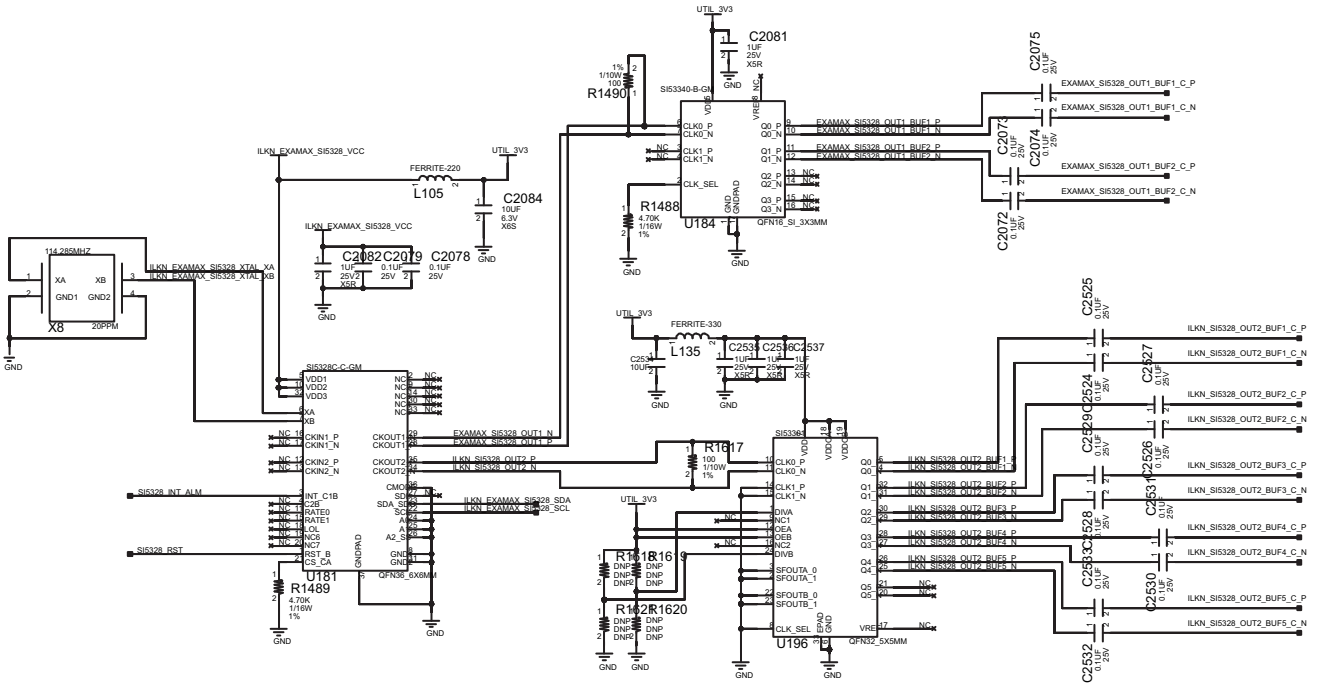

Figure 1-12: **ExaMAX and Interlaken Connector Interface Jitter-Attenuating Clock Multiplier**

This SI5328C U181 ExaMAX and Interlaken connector clock multiplier is used to generate the multiple clock frequencies required to drive these two connector interfaces.

User SMA Clock

[Figure 1-2, callout 15]

The VCU110 evaluation board provides an SMA pair for the user to source a differential LVDS clock to FPGA U1 bank 67. USER_SMA_CLOCK_P and USER_SMA_CLOCK_N are connected to XCVU190 FPGA U1 (V_{CCO} 1.5V) HP bank 67 GC pins AY27 and AY28, respectively. A 100Ω differential termination resistor is present on the board for these inputs.

The SMA input circuit is shown in Figure 1-13.

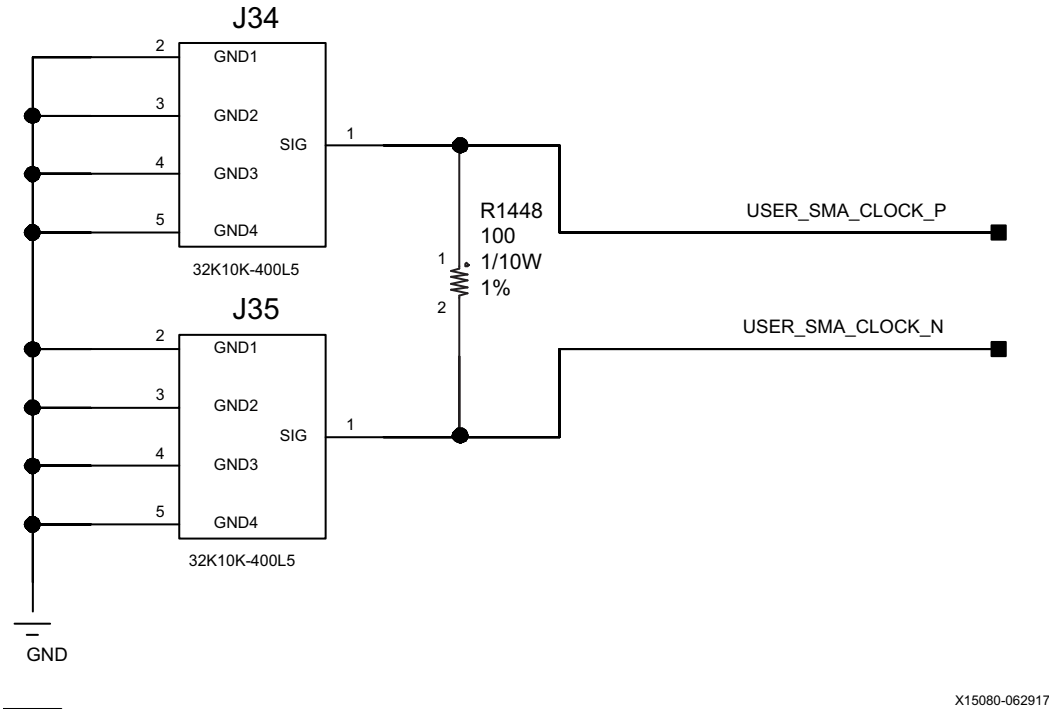

Figure 1-13: **VCU110 User SMA Clock**

GTY Transceivers

[Figure 1-2, callout 2]

The GTY transceivers in the XCVU190 are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTY Quad of interest. There are thirteen GTY Quads (banks 120-132) on the VCU110 board with connectivity as shown below:

The VCU110 board provides access to 13 of 13 GTY transceiver Quads:

- Two of the GTY Quads, banks 120-121 are connected to ExaMAX connector J116.
- Four of the GTY Quads, banks 122, 125, 127, and 128 are connected to CFP4 connectors J107, J108, J109, and J110, respectively.
- Two of the GTY Quads, banks 124 and 126 are connected to BullsEye connectors J122 (BULLSEYE2) and J87 (BULLSEYE1), respectively.
- Five of the GTY Quads, banks 129-133 are connected to Interlaken connector J131.

Quad 120:

- REFCLK0 - EXAMAX_SI5328_OUT1_BUF1_C_P/N (U184)
- REFCLK1 - not connected
- Four GTY transceivers allocated to EXAMAX_TX/RX[5:8]_P/N (J116)

Quad 121:

- REFCLK0 - EXAMAX_SI5328_OUT1_BUF2_C_P/N (U184)
- REFCLK1 - not connected
- Four GTY transceivers allocated to EXAMAX_TX/RX[1:4]_P/N (J116)

Quad 122:

- REFCLK0 - CFP4_SI5328_OUT1_BUF1_C_P/N (U180)
- REFCLK1 - not connected
- Four GTY transceivers allocated to CFP4_MOD0_TX/RX[0:3]_P/N (J107)

Quad 124:

- REFCLK0 - BULLSEYE2_GTY_REFCLK0_C_P/N (J122)
- REFCLK1 - BULLSEYE2_GTY_REFCLK1_C_P/N (J122)
- Four GTY transceivers allocated to BULLSEYE2_GTY_TX/RX[0:3]_P/N (J122)

Quad 125:

- REFCLK0 - CFP4_SI5328_OUT1_BUF2_C_P/N (U180)
- REFCLK1 - not connected
- Four GTY transceivers allocated to CFP4_MOD1_TX/RX[0:3]_P/N (J108)

Quad 126:

- REFCLK0 - BULLSEYE1_GTY_REFCLK0_C_P/N (J87)
- REFCLK1 - BULLSEYE1_GTY_REFCLK1_C_P/N (J87)
- Four GTY transceivers allocated to BULLSEYE1_GTY_TX/RX[0:3]_P/N (J87)

Quad 127:

- REFCLK0 - CFP4_SI5328_OUT1_BUF3_C_P/N (U180)
- REFCLK1 - not connected
- Four GTY transceivers allocated to CFP4_MOD2_TX/RX[0:3]_P/N (J109)

Quad 128:

- REFCLK0 - CFP4_SI5328_OUT1_BUF4_C_P/N (U180)
- REFCLK1 - CFP4_REC_CLOCK2_C_P/N (U179)
- Four GTY transceivers allocated to CFP4_MOD3_TX/RX[0:3]_P/N (J110)

Quad 129:

- REFCLK0 - ILKN_SI5328_OUT2_BUF1_C_P/N (U196)
- REFCLK1 - not connected
- Four GTY transceivers allocated to ILKN_TX/RX[0:3]_P/N (J121)

Quad 130:

- REFCLK0 - ILKN_SI5328_OUT2_BUF2_C_P/N (U196)
- REFCLK1 - not connected
- Four GTY transceivers allocated to ILKN_TX/RX[4:7]_P/N (J121)

Quad 131:

- REFCLK0 - ILKN_SI5328_OUT2_BUF3_C_P/N (U196)
- REFCLK1 - not connected
- Four GTY transceivers allocated to ILKN_TX/RX[8:11]_P/N (J121)

Quad 132:

- REFCLK0 - ILKN_SI5328_OUT2_BUF4_C_P/N (U196)
- REFCLK1 - not connected
- Four GTY transceivers allocated to ILKN_TX/RX[12:15]_P/N (J121)

Quad 133:

- REFCLK0 - ILKN_SI5328_OUT2_BUF5_C_P/N (U196)
- REFCLK1 - not connected
- Four GTY transceivers allocated to ILKN_TX/RX[16:19]_P/N (J121)

Table 1-13 through Table 1-25 below list the VCU110 FPGA U1 GTY bank 120-122 and 124-133 connections, respectively.

Table 1-13: **VCU110 FPGA U1 GTY Quad 120 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_120	BF38	EXAMAX_TX8_P	I7	TX8_P	ExaMAX J116
MGTYTXN0_120	BF39	EXAMAX_TX8_N	J7	TX8_N	
MGTYRXP0_120	BF33	EXAMAX_RX8_P	F7	RX8_P	
MGTYRXN0_120	BF34	EXAMAX_RX8_N	G7	RX8_N	
MGTYTXP1_120	BE36	EXAMAX_TX7_P	L7	TX7_P	
MGTYTXN1_120	BE37	EXAMAX_TX7_N	M7	TX7_N	
MGTYRXP1_120	BD33	EXAMAX_RX7_P	C7	RX7_P	
MGTYRXN1_120	BD34	EXAMAX_RX7_N	D7	RX7_N	
MGTYTXP2_120	BE40	EXAMAX_TX6_P	H6	TX6_P	
MGTYTXN2_120	BE41	EXAMAX_TX6_N	I6	TX6_N	
MGTYRXP2_120	BF43	EXAMAX_RX6_P	E6	RX6_P	
MGTYRXN2_120	BF44	EXAMAX_RX6_N	F6	RX6_N	
MGTYTXP3_120	BD38	EXAMAX_TX5_P	K6	TX5_P	
MGTYTXN3_120	BD39	EXAMAX_TX5_N	L6	TX5_N	
MGTYRXP3_120	BD43	EXAMAX_RX5_P	B6	RX5_P	
MGTYRXN3_120	BD44	EXAMAX_RX5_N	C6	RX5_N	
MGTREFCLK0P_120	AN36	EXAMAX_SI5328_OUT1_BUF1_C_P[2]	28	CKOUT1_P	SI5328 U181
MGTREFCLK0N_120	AN37	EXAMAX_SI5328_OUT1_BUF1_C_N[2]	29	CKOUT1_N	
MGTREFCLK1P_120	AM34	NA	NA	NA	NA
MGTREFCLK1N_120	AM35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-14: **VCU110 FPGA U1 GTY Quad 121 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_121	BC40	EXAMAX_TX4_P	I5	TX4_P	ExaMAX J116
MGTYTXN0_121	BC41	EXAMAX_TX4_N	J5	TX4_N	
MGTYRXP0_121	BC45	EXAMAX_RX4_P	F5	RX4_P	
MGTYRXN0_121	BC46	EXAMAX_RX4_N	G5	RX4_N	
MGTYTXP1_121	BB38	EXAMAX_TX3_P	L5	TX3_P	
MGTYTXN1_121	BB39	EXAMAX_TX3_N	M5	TX3_N	
MGTYRXP1_121	BB43	EXAMAX_RX3_P	C5	RX3_P	
MGTYRXN1_121	BB44	EXAMAX_RX3_N	D5	RX3_N	
MGTYTXP2_121	BA40	EXAMAX_TX2_P	H4	TX2_P	
MGTYTXN2_121	BA41	EXAMAX_TX2_N	I4	TX2_N	
MGTYRXP2_121	BA45	EXAMAX_RX2_P	E4	RX2_P	
MGTYRXN2_121	BA46	EXAMAX_RX2_N	F4	RX2_N	
MGTYTXP3_121	AY38	EXAMAX_TX1_P	K4	TX1_P	
MGTYTXN3_121	AY39	EXAMAX_TX1_N	L4	TX1_N	
MGTYRXP3_121	AY43	EXAMAX_RX1_P	B4	RX1_P	
MGTYRXN3_121	AY44	EXAMAX_RX1_N	C4	RX1_N	
MGTREFCLK0P_121	AL36	EXAMAX_SI5328_OUT1_BUF2_C_P[2]	28	CKOUT_P	SI5328 U181
MGTREFCLK0N_121	AL37	EXAMAX_SI5328_OUT1_BUF2_C_N[2]	29	CKOUT_N	
MGTREFCLK1P_121	AK34	NA	NA	NA	NA
MGTREFCLK1N_121	AK35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-15: **VCU110 FPGA U1 GTY Quad 122 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_122	AW40	CFP4_MOD0_TX3_P	54	TX3P--TX0P	CFP4 MOD0 J107
MGTYTXN0_122	AW41	CFP4_MOD0_TX3_N	55	TX3N--TX0N	
MGTYRXP0_122	AW45	CFP4_MOD0_RX3_P	39	RX3P--RX3N	
MGTYRXN0_122	AW46	CFP4_MOD0_RX3_N	40	RX3N--RX3P	
MGTYTXP1_122	AV38	CFP4_MOD0_TX2_P	51	TX2P--TX1P	
MGTYTXN1_122	AV39	CFP4_MOD0_TX2_N	52	TX2N--TX1N	
MGTYRXP1_122	AV43	CFP4_MOD0_RX2_P	36	RX2P--RX2N	
MGTYRXN1_122	AV44	CFP4_MOD0_RX2_N	37	RX2N--RX2P	
MGTYTXP2_122	AU40	CFP4_MOD0_TX1_P	48	TX1P--TX2P	
MGTYTXN2_122	AU41	CFP4_MOD0_TX1_N	49	TX1N--TX2N	
MGTYRXP2_122	AU45	CFP4_MOD0_RX1_P	33	RX1P--RX1N	
MGTYRXN2_122	AU46	CFP4_MOD0_RX1_N	34	RX1N--RX1P	
MGTYTXP3_122	AT38	CFP4_MOD0_TX0_P	45	TX0P--TX3P	
MGTYTXN3_122	AT39	CFP4_MOD0_TX0_N	46	TX0N--TX3N	
MGTYRXP3_122	AT43	CFP4_MOD0_RX0_P	30	RX0N--RX0P	
MGTYRXN3_122	AT44	CFP4_MOD0_RX0_N	31	RX0P--RX0N	
MGTREFCLK0P_122	AJ36	CFP4_SI5328_OUT1_BUF1_C_P[2]	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_122	AJ37	CFP4_SI5328_OUT1_BUF1_C_N[2]	29	CKOUT1_N	
MGTREFCLK1P_122	AH34	NA	NA	NA	NA
MGTREFCLK1N_122	AH35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-16: **VCU110 FPGA U1 GTY Quad 124 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_124	AR40	BULLSEYE2_GTY_TX0_P	15	P15	BULLSEYE2 J122
MGTYTXN0_124	AR41	BULLSEYE2_GTY_TX0_N	16	P16	
MGTYRXP0_124	AR45	BULLSEYE2_GTY_RX0_P	17	P17	
MGTYRXN0_124	AR46	BULLSEYE2_GTY_RX0_N	18	P18	
MGTYTXP1_124	AP38	BULLSEYE2_GTY_TX1_P	13	P13	
MGTYTXN1_124	AP39	BULLSEYE2_GTY_TX1_N	14	P14	
MGTYRXP1_124	AP43	BULLSEYE2_GTY_RX1_P	11	P11	
MGTYRXN1_124	AP44	BULLSEYE2_GTY_RX1_N	12	P12	
MGTYTXP2_124	AN40	BULLSEYE2_GTY_TX2_P	7	P7	
MGTYTXN2_124	AN41	BULLSEYE2_GTY_TX2_N	8	P8	
MGTYRXP2_124	AN45	BULLSEYE2_GTY_RX2_P	9	P9	
MGTYRXN2_124	AN46	BULLSEYE2_GTY_RX2_N	10	P10	
MGTYTXP3_124	AM38	BULLSEYE2_GTY_TX3_P	5	P5	
MGTYTXN3_124	AM39	BULLSEYE2_GTY_TX3_N	6	P6	
MGTYRXP3_124	AM43	BULLSEYE2_GTY_RX3_P	3	P3	
MGTYRXN3_124	AM44	BULLSEYE2_GTY_RX3_N	4	P4	
MGTREFCLK0P_124	AG36	BULLSEYE2_GTY_REFCLK0_C_P[2]	19	P19	
MGTREFCLK0N_124	AG37	BULLSEYE2_GTY_REFCLK0_C_N[2]	20	P20	
MGTREFCLK1P_124	AF34	BULLSEYE2_GTY_REFCLK1_C_P[2]	1	P1	
MGTREFCLK1N_124	AF35	BULLSEYE2_GTY_REFCLK1_C_N[2]	2	P2	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-17: **VCU110 FPGA U1 GTY Quad 125 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_125	AL40	CFP4_MOD1_TX3_P	54	TX3P--TX0P	CFP4 MOD1 J108
MGTYTXN0_125	AL41	CFP4_MOD1_TX3_N	55	TX3N--TX0N	
MGTYRXP0_125	AL45	CFP4_MOD1_RX3_P	39	RX3P--RX3N	
MGTYRXN0_125	AL46	CFP4_MOD1_RX3_N	40	RX3N--RX3P	
MGTYTXP1_125	AK38	CFP4_MOD1_TX2_P	51	TX2P--TX1P	
MGTYTXN1_125	AK39	CFP4_MOD1_TX2_N	52	TX2N--TX1N	
MGTYRXP1_125	AK43	CFP4_MOD1_RX2_P	36	RX2P--RX2N	
MGTYRXN1_125	AK44	CFP4_MOD1_RX2_N	37	RX2N--RX2P	
MGTYTXP2_125	AJ40	CFP4_MOD1_TX1_P	48	TX1P--TX2P	
MGTYTXN2_125	AJ41	CFP4_MOD1_TX1_N	49	TX1N--TX2N	
MGTYRXP2_125	AJ45	CFP4_MOD1_RX1_P	33	RX1P--RX1N	
MGTYRXN2_125	AJ46	CFP4_MOD1_RX1_N	34	RX1N--RX1P	
MGTYTXP3_125	AH38	CFP4_MOD1_TX0_P	45	TX0P--TX3P	
MGTYTXN3_125	AH39	CFP4_MOD1_TX0_N	46	TX0N--TX3N	
MGTYRXP3_125	AH43	CFP4_MOD1_RX0_P	30	RX0N--RX0P	
MGTYRXN3_125	AH44	CFP4_MOD1_RX0_N	31	RX0P--RX0N	
MGTREFCLK0P_125	AE36	CFP4_SI5328_OUT1_BUF2_C_P[2]	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_125	AE37	CFP4_SI5328_OUT1_BUF2_C_N[2]	29	CKOUT1_N	
MGTREFCLK1P_125	AD34	NA	NA	NA	NA
MGTREFCLK1N_125	AD35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-18: **VCU110 FPGA U1 GTY Quad 126 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_126	AG40	BULLSEYE1_GTY_TX0_P	15	P15	BULLSEYE1 J87
MGTYTXN0_126	AG41	BULLSEYE1_GTY_TX0_N	16	P16	
MGTYRXP0_126	AG45	BULLSEYE1_GTY_RX0_P	17	P17	
MGTYRXN0_126	AG46	BULLSEYE1_GTY_RX0_N	18	P18	
MGTYTXP1_126	AF38	BULLSEYE1_GTY_TX1_P	13	P13	
MGTYTXN1_126	AF39	BULLSEYE1_GTY_TX1_N	14	P14	
MGTYRXP1_126	AF43	BULLSEYE1_GTY_RX1_P	11	P11	
MGTYRXN1_126	AF44	BULLSEYE1_GTY_RX1_N	12	P12	
MGTYTXP2_126	AE40	BULLSEYE1_GTY_TX2_P	7	P7	
MGTYTXN2_126	AE41	BULLSEYE1_GTY_TX2_N	8	P8	
MGTYRXP2_126	AE45	BULLSEYE1_GTY_RX2_P	9	P9	
MGTYRXN2_126	AE46	BULLSEYE1_GTY_RX2_N	10	P10	
MGTYTXP3_126	AD38	BULLSEYE1_GTY_TX3_P	5	P5	
MGTYTXN3_126	AD39	BULLSEYE1_GTY_TX3_N	6	P6	
MGTYRXP3_126	AD43	BULLSEYE1_GTY_RX3_P	3	P3	
MGTYRXN3_126	AD44	BULLSEYE1_GTY_RX3_N	4	P4	
MGTREFCLK0P_126	AC36	BULLSEYE1_GTY_REFCLK0_C_P[2]	19	P19	
MGTREFCLK0N_126	AC37	BULLSEYE1_GTY_REFCLK0_C_N[2]	20	P20	
MGTREFCLK1P_126	AB34	BULLSEYE1_GTY_REFCLK1_C_P[2]	1	P1	
MGTREFCLK1N_126	AB35	BULLSEYE1_GTY_REFCLK1_C_N[2]	2	P2	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-19: **VCU110 FPGA U1 GTY Quad 127 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name (1)	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_127	AC40	CFP4_MOD2_TX3_P	54	TX3P--TX0P	CFP4 MOD2 J109
MGTYTXN0_127	AC41	CFP4_MOD2_TX3_N	55	TX3N--TX0N	
MGTYRXP0_127	AC45	CFP4_MOD2_RX3_P	39	RX3P--RX3N	
MGTYRXN0_127	AC46	CFP4_MOD2_RX3_N	40	RX3N--RX3P	
MGTYTXP1_127	AB38	CFP4_MOD2_TX2_P	51	TX2P--TX1P	
MGTYTXN1_127	AB39	CFP4_MOD2_TX2_N	52	TX2N--TX1N	
MGTYRXP1_127	AB43	CFP4_MOD2_RX2_P	36	RX2P--RX2N	
MGTYRXN1_127	AB44	CFP4_MOD2_RX2_N	37	RX2N--RX2P	
MGTYTXP2_127	AA40	CFP4_MOD2_TX1_P	48	TX1P--TX2P	
MGTYTXN2_127	AA41	CFP4_MOD2_TX1_N	49	TX1N--TX2N	
MGTYRXP2_127	AA45	CFP4_MOD2_RX1_P	33	RX1P--RX1N	
MGTYRXN2_127	AA46	CFP4_MOD2_RX1_N	34	RX1N--RX1P	
MGTYTXP3_127	Y38	CFP4_MOD2_TX0_P	45	TX0P--TX3P	
MGTYTXN3_127	Y39	CFP4_MOD2_TX0_N	46	TX0N--TX3N	
MGTYRXP3_127	Y43	CFP4_MOD2_RX0_P	30	RX0N--RX0P	
MGTYRXN3_127	Y44	CFP4_MOD2_RX0_N	31	RX0P--RX0N	
MGTREFCLK0P_127	AA36	CFP4_SI5328_OUT1_BUF3_C_P(2)	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_127	AA37	CFP4_SI5328_OUT1_BUF3_C_N(2)	29	CKOUT1_N	
MGTREFCLK1P_127	Y34	NA	NA	NA	NA
MGTREFCLK1N_127	Y35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-20: **VCU110 FPGA U1 GTY Quad 128 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_128	W40	CFP4_MOD3_TX3_P	54	TX3P--TX0P	CFP4 MOD3 J110
MGTYTXN0_128	W41	CFP4_MOD3_TX3_N	55	TX3N--TX0N	
MGTYRXP0_128	W45	CFP4_MOD3_RX3_P	39	RX3P--RX3N	
MGTYRXN0_128	W46	CFP4_MOD3_RX3_N	40	RX3N--RX3P	
MGTYTXP1_128	V38	CFP4_MOD3_TX2_P	51	TX2P--TX1P	
MGTYTXN1_128	V39	CFP4_MOD3_TX2_N	52	TX2N--TX1N	
MGTYRXP1_128	V43	CFP4_MOD3_RX2_P	36	RX2P--RX2N	
MGTYRXN1_128	V44	CFP4_MOD3_RX2_N	37	RX2N--RX2P	
MGTYTXP2_128	U40	CFP4_MOD3_TX1_P	48	TX1P--TX2P	
MGTYTXN2_128	U41	CFP4_MOD3_TX1_N	49	TX1N--TX2N	
MGTYRXP2_128	U45	CFP4_MOD3_RX1_P	33	RX1P--RX1N	
MGTYRXN2_128	U46	CFP4_MOD3_RX1_N	34	RX1N--RX1P	
MGTYTXP3_128	T38	CFP4_MOD3_TX0_P	45	TX0P--TX3P	
MGTYTXN3_128	T39	CFP4_MOD3_TX0_N	46	TX0N--TX3N	
MGTYRXP3_128	T43	CFP4_MOD3_RX0_P	30	RX0N--RX0P	
MGTYRXN3_128	T44	CFP4_MOD3_RX0_N	31	RX0P--RX0N	
MGTREFCLK0P_128	W36	CFP4_SI5328_OUT1_BUF4_C_P[2]	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_128	W37	CFP4_SI5328_OUT1_BUF4_C_N[2]	29	CKOUT1_N	
MGTREFCLK1P_128	V34	CFP4_REC_CLOCK2_C_P(1)	12	CKIN2_P	SI5328 U179
MGTREFCLK1N_128	V35	CFP4_REC_CLOCK2_C_N(1)	13	CKIN2_N	

Notes:

1. MGT connections I/O standard not applicable
2. Series capacitor coupled

Table 1-21: **VCU110 FPGA U1 GTY Quad 129 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_129	R40	ILKN_TX0_P	A2	TX0_P	Interlaken J121
MGTYTXN0_129	R41	ILKN_TX0_N	A3	TX0_N	
MGTYRXP0_129	R45	ILKN_RX0_C_P[2]	B2	RX0_P	
MGTYRXN0_129	R46	ILKN_RX0_C_N[2]	B3	RX0_N	
MGTYTXP1_129	P38	ILKN_TX1_P	C2	TX1_P	
MGTYTXN1_129	P39	ILKN_TX1_N	C3	TX1_N	
MGTYRXP1_129	P43	ILKN_RX1_C_P[2]	D2	RX1_P	
MGTYRXN1_129	P44	ILKN_RX1_C_N[2]	D3	RX1_N	
MGTYTXP2_129	N40	ILKN_TX2_P	A5	TX2_P	
MGTYTXN2_129	N41	ILKN_TX2_N	A6	TX2_N	
MGTYRXP2_129	N45	ILKN_RX2_C_P[2]	B5	RX2_P	
MGTYRXN2_129	N46	ILKN_RX2_C_N[2]	B6	RX2_N	
MGTYTXP3_129	M38	ILKN_TX3_P	C5	TX3_P	
MGTYTXN3_129	M39	ILKN_TX3_N	C6	TX3_N	
MGTYRXP3_129	M43	ILKN_RX3_C_P[2]	D5	RX3_P	
MGTYRXN3_129	M44	ILKN_RX3_C_N[2]	D6	RX3_N	
MGTREFCLK0P_129	U36	ILKN_SI5328_OUT2_BUF1_C_P[2]	35	CKOUT2_P	SI5328 U181
MGTREFCLK0N_129	U37	ILKN_SI5328_OUT2_BUF1_C_N[2]	34	CKOUT2_N	
MGTREFCLK1P_129	T34	NA	NA	NA	NA
MGTREFCLK1N_129	T35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-22: **VCU110 FPGA U1 GTY Quad 130 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_130	L40	ILKN_TX4_P	A8	TX4_P	Interlaken J121
MGTYTXN0_130	L41	ILKN_TX4_N	A9	TX4_N	
MGTYRXP0_130	L45	ILKN_RX4_C_P[2]	B8	RX4_P	
MGTYRXN0_130	L46	ILKN_RX4_C_N[2]	B9	RX4_N	
MGTYTXP1_130	K38	ILKN_TX5_P	C8	TX5_P	
MGTYTXN1_130	K39	ILKN_TX5_N	C9	TX5_N	
MGTYRXP1_130	K43	ILKN_RX5_C_P[2]	D8	RX5_P	
MGTYRXN1_130	K44	ILKN_RX5_C_N[2]	D9	RX5_N	
MGTYTXP2_130	J40	ILKN_TX6_P	F2	TX6_P	
MGTYTXN2_130	J41	ILKN_TX6_N	F3	TX6_N	
MGTYRXP2_130	J45	ILKN_RX6_C_P[2]	G2	RX6_P	
MGTYRXN2_130	J46	ILKN_RX6_C_N[2]	G3	RX6_N	
MGTYTXP3_130	H38	ILKN_TX7_P	H2	TX7_P	
MGTYTXN3_130	H39	ILKN_TX7_N	H3	TX7_N	
MGTYRXP3_130	H43	ILKN_RX7_C_P[2]	J2	RX7_P	
MGTYRXN3_130	H44	ILKN_RX7_C_N[2]	J3	RX7_N	
MGTREFCLK0P_130	R36	ILKN_SI5328_OUT2_BUF2_C_P[2]	35	CKOUT2_P	SI5328 U181
MGTREFCLK0N_130	R37	ILKN_SI5328_OUT2_BUF2_C_N[2]	34	CKOUT2_N	
MGTREFCLK1P_130	P34	NA	NA	NA	NA
MGTREFCLK1N_130	P35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-23: **VCU110 FPGA U1 GTY Quad 131 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_131	G40	ILKN_TX8_P	F5	TX8_P	Interlaken J121
MGTYTXN0_131	G41	ILKN_TX8_N	F6	TX8_N	
MGTYRXP0_131	G45	ILKN_RX8_C_P[2]	G5	RX8_P	
MGTYRXN0_131	G46	ILKN_RX8_C_N[2]	G6	RX8_N	
MGTYTXP1_131	F38	ILKN_TX9_P	H5	TX9_P	
MGTYTXN1_131	F39	ILKN_TX9_N	H6	TX9_N	
MGTYRXP1_131	F43	ILKN_RX9_C_P[2]	J5	RX9_P	
MGTYRXN1_131	F44	ILKN_RX9_C_N[2]	J6	RX9_N	
MGTYTXP2_131	G36	ILKN_TX10_P	F8	TX10_P	
MGTYTXN2_131	G37	ILKN_TX10_N	F9	TX10_N	
MGTYRXP2_131	G31	ILKN_RX10_C_P[2]	G8	RX10_P	
MGTYRXN2_131	G32	ILKN_RX10_C_N[2]	G9	RX10_N	
MGTYTXP3_131	F34	ILKN_TX11_P	H8	TX11_P	
MGTYTXN3_131	F35	ILKN_TX11_N	H9	TX11_N	
MGTYRXP3_131	E31	ILKN_RX11_C_P[2]	J8	RX11_P	
MGTYRXN3_131	E32	ILKN_RX11_C_N[2]	J9	RX11_N	
MGTREFCLK0P_131	N36	ILKN_SI5328_OUT2_BUF3_C_P[2]	35	CKOUT2_P	SI5328 U181
MGTREFCLK0N_131	N37	ILKN_SI5328_OUT2_BUF3_C_N[2]	34	CKOUT2_N	
MGTREFCLK1P_131	M34	NA	NA	NA	NA
MGTREFCLK1N_131	M35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-24: **VCU110 FPGA U1 GTY Quad 132 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_132	E40	ILKN_TX12_P	F11	TX12_P	Interlaken J121
MGTYTXN0_132	E41	ILKN_TX12_N	F12	TX12_N	
MGTYRXP0_132	E45	ILKN_RX12_C_P[2]	G11	RX12_P	
MGTYRXN0_132	E46	ILKN_RX12_C_N[2]	G12	RX12_N	
MGTYTXP1_132	E36	ILKN_TX13_P	H11	TX13_P	
MGTYTXN1_132	E37	ILKN_TX13_N	H12	TX13_N	
MGTYRXP1_132	D43	ILKN_RX13_C_P[2]	J11	RX13_P	
MGTYRXN1_132	D44	ILKN_RX13_C_N[2]	J12	RX13_N	
MGTYTXP2_132	C40	ILKN_TX14_P	F14	TX14_P	
MGTYTXN2_132	C41	ILKN_TX14_N	F15	TX14_N	
MGTYRXP2_132	C45	ILKN_RX14_C_P[2]	J14	RX14_P	
MGTYRXN2_132	C46	ILKN_RX14_C_N[2]	J15	RX14_N	
MGTYTXP3_132	A40	ILKN_TX15_P	H14	TX15_P	
MGTYTXN3_132	A41	ILKN_TX15_N	H15	TX15_N	
MGTYRXP3_132	B43	ILKN_RX15_C_P[2]	J14	RX15_P	
MGTYRXN3_132	B44	ILKN_RX15_C_N[2]	J15	RX15_N	
MGTREFCLK0P_132	L36	ILKN_SI5328_OUT2_BUF4_C_P[2]	35	CKOUT2_P	SI5328 U181
MGTREFCLK0N_132	L37	ILKN_SI5328_OUT2_BUF4_C_N[2]	34	CKOUT2_N	
MGTREFCLK1P_132	K34	NA	NA	NA	NA
MGTREFCLK1N_132	K35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-25: **VCU110 FPGA U1 GTY Quad 133 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_133	D38	ILKN_TX16_P	A11	TX16_P	Interlaken J121
MGTYTXN0_133	D39	ILKN_TX16_N	A12	TX16_N	
MGTYRXP0_133	D33	ILKN_RX16_C_P[2]	J14	RX16_P	
MGTYRXN0_133	D34	ILKN_RX16_C_N[2]	J15	RX16_N	
MGTYTXP1_133	C36	ILKN_TX17_P	C11	TX17_P	
MGTYTXN1_133	C37	ILKN_TX17_N	C12	TX17_N	
MGTYRXP1_133	C31	ILKN_RX17_C_P[2]	D11	RX17_P	
MGTYRXN1_133	C32	ILKN_RX17_C_N[2]	D12	RX17_N	
MGTYTXP2_133	B38	ILKN_TX18_P	A14	TX18_P	
MGTYTXN2_133	B39	ILKN_TX18_N	A15	TX18_N	
MGTYRXP2_133	B33	ILKN_RX18_C_P[2]	B14	RX18_P	
MGTYRXN2_133	B34	ILKN_RX18_C_N[2]	B15	RX18_N	
MGTYTXP3_133	A36	ILKN_TX19_P	C14	TX19_P	
MGTYTXN3_133	A37	ILKN_TX19_N	C15	TX19_N	
MGTYRXP3_133	A31	ILKN_RX19_C_P[2]	D14	RX19_P	
MGTYRXN3_133	A32	ILKN_RX19_C_N[2]	D15	RX19_N	
MGTREFCLK0P_133	J36	ILKN_SI5328_OUT2_BUF5_C_P[2]	35	CKOUT2_P	SI5328 U181
MGTREFCLK0N_133	J37	ILKN_SI5328_OUT2_BUF5_C_N[2]	34	CKOUT2_N	
MGTREFCLK1P_133	H34	NA	NA	NA	NA
MGTREFCLK1N_133	H35	NA	NA	NA	

Notes:
1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

For additional information on GTH transceivers, see *UltraScale Architecture GTY Transceivers User Guide* (UG578) [Ref 5].

Also see *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182) [Ref 6].

GTH Transceivers

[Figure 1-2, callout 3]

The VCU110 board provides access to 13 of 13 GTH transceiver Quads:

- Two of the GTH Quads are wired to the FMC HPC0 connector (J22)
- Two of the GTH Quads are wired to the FMC HPC1 connector (J2)

- Eight of the GTH Quads are wired to the HMC device (U160)
- One of the GTH Quads is wired to the PCIe cable connector J136

The GTH transceivers in the XCVU190 are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTH Quad of interest. There are thirteen GTH Quads (banks 220-232) on the VCU110 board, with connectivity as shown here:

Quad 220:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to FMC_HPC0_DP[0:3]_C2M and M2C_P/N (J22)

Quad 221:

- REFCLK0 - FMC_HPC0_GBTCLK0_M2C_C_P/N (J22)
- REFCLK1 - FMC_HPC0_GBTCLK1_M2C_C_P/N (J22)
- Four GTH transceivers allocated to FMC_HPC0_DP[4:7]_C2M and M2C_P/N (J22)

Quad 222:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to FMC_HPC1_DP[4:7]_C2M and M2C_P/N (J2)

Quad 224:

- REFCLK0 - FMC_HPC1_GBTCLK0_M2C_C_P/N (J2)
- REFCLK1 - FMC_HPC1_GBTCLK1_M2C_C_P/N (J2)
- Four GTH transceivers allocated to FMC_HPC1_DP[0:3]_C2M and M2C_P/N (J2)

Quad 225:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to HMC_L1 TX and RX[0,1,2,6]_P/N (U160)

Quad 226:

- REFCLK0 - HMC_SI5328_OUT2_BUF2_C_P/N (U165)
- REFCLK1 - not connected

- Four GTH transceivers allocated to HMC_L1 TX and RX[3,4,5,7]_P/N (U160)

Quad 227:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to HMC_L1 TX and RX[11,13,14,15]_P/N (U160)

Quad 228:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to HMC_L1 TX and RX[8,9,10,12]_P/N (U160)

Quad 229:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to HMC_L0 TX and RX[8,9,12,13]_P/N (U160)

Quad 230:

- REFCLK0 - HMC_SI5328_OUT2_BUF1_C_P/N (U165)
- REFCLK1 - not connected
- Four GTH transceivers allocated to HMC_L0 TX and RX[0,1,10,14]_P/N (U160)

Quad 231:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to HMC_L0 TX and RX[2,4,6,11]_P/N (U160)

Quad 232:

- REFCLK0 - not connected
- REFCLK1 - not connected
- Four GTH transceivers allocated to HMC_L0 TX and RX[12:15]_P/N (U160)

Quad 233:

- REFCLK0 - PCIE_CABLE_CLK_C_P/N (J136)
- REFCLK1 - not connected

- Four GTH transceivers allocated to PCIE_CABLE_TX and RX[0:3]_P/N (J136)

Table 1-26 through Table 1-38 list the VCU110 FPGA U1 GTH Quads 220-222 and 224-233 connections, respectively.

Table 1-26: **VCU110 FPGA U1 GTH Quad 220 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name(1)	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_220	BF9	FMC_HPC0_DP0_C2M_P	C2	DP0_C2M_P	FMC HPC0 J22
MGTHTXN0_220	BF8	FMC_HPC0_DP0_C2M_N	C3	DP0_C2M_N	
MGTHRXP0_220	BF14	FMC_HPC0_DP0_M2C_P	C6	DP0_M2C_P	
MGTHRXN0_220	BF13	FMC_HPC0_DP0_M2C_N	C7	DP0_M2C_N	
MGTHTXP1_220	BE11	FMC_HPC0_DP1_C2M_P	A22	DP1_C2M_P	
MGTHTXN1_220	BE10	FMC_HPC0_DP1_C2M_N	A23	DP1_C2M_N	
MGTHRXP1_220	BD14	FMC_HPC0_DP1_M2C_P	A2	DP1_M2C_P	
MGTHRXN1_220	BD13	FMC_HPC0_DP1_M2C_N	A3	DP1_M2C_N	
MGTHTXP2_220	BE7	FMC_HPC0_DP2_C2M_P	A26	DP2_C2M_P	
MGTHTXN2_220	BE6	FMC_HPC0_DP2_C2M_N	A27	DP2_C2M_N	
MGTHRXP2_220	BF4	FMC_HPC0_DP2_M2C_P	A6	DP2_M2C_P	
MGTHRXN2_220	BF3	FMC_HPC0_DP2_M2C_N	A7	DP2_M2C_N	
MGTHTXP3_220	BD9	FMC_HPC0_DP3_C2M_P	A30	DP3_C2M_P	
MGTHTXN3_220	BD8	FMC_HPC0_DP3_C2M_N	A31	DP3_C2M_N	
MGTHRXP3_220	BD4	FMC_HPC0_DP3_M2C_P	A10	DP3_M2C_P	
MGTHRXN3_220	BD3	FMC_HPC0_DP3_M2C_N	A11	DP3_M2C_N	
MGTREFCLK0P_220	AN11	NA	NA	NA	NA
MGTREFCLK0N_220	AN10	NA	NA	NA	
MGTREFCLK1P_220	AM13	NA	NA	NA	
MGTREFCLK1N_220	AM12	NA	NA	NA	

Notes:
1. MGT connections I/O standard not applicable.

Table 1-27: **VCU110 FPGA U1 GTH Quad 221 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_221	BC7	FMC_HPC0_DP4_C2M_P	A34	DP4_C2M_P	FMC HPC0 J22
MGTHTXN0_221	BC6	FMC_HPC0_DP4_C2M_N	A35	DP4_C2M_N	
MGTHRXP0_221	BC2	FMC_HPC0_DP4_M2C_P	A14	DP4_M2C_P	
MGTHRXN0_221	BC1	FMC_HPC0_DP4_M2C_N	A15	DP4_M2C_N	
MGTHTXP1_221	BB9	FMC_HPC0_DP5_C2M_P	A38	DP5_C2M_P	
MGTHTXN1_221	BB8	FMC_HPC0_DP5_C2M_N	A39	DP5_C2M_N	
MGTHRXP1_221	BB4	FMC_HPC0_DP5_M2C_P	A18	DP5_M2C_P	
MGTHRXN1_221	BB3	FMC_HPC0_DP5_M2C_N	A19	DP5_M2C_N	
MGTHTXP2_221	BA7	FMC_HPC0_DP6_C2M_P	B36	DP6_C2M_P	
MGTHTXN2_221	BA6	FMC_HPC0_DP6_C2M_N	B37	DP6_C2M_N	
MGTHRXP2_221	BA2	FMC_HPC0_DP6_M2C_P	B16	DP6_M2C_P	
MGTHRXN2_221	BA1	FMC_HPC0_DP6_M2C_N	B17	DP6_M2C_N	
MGTHTXP3_221	AY9	FMC_HPC0_DP7_C2M_P	B32	DP7_C2M_P	
MGTHTXN3_221	AY8	FMC_HPC0_DP7_C2M_N	B33	DP7_C2M_N	
MGTHRXP3_221	AY4	FMC_HPC0_DP7_M2C_P	B12	DP7_M2C_P	
MGTHRXN3_221	AY3	FMC_HPC0_DP7_M2C_N	B13	DP7_M2C_N	
MGTREFCLK0P_221	AL11	FMC_HPC0_GBTCLK0_M2C_C_P[2]	D4	GBTCLK0_ M2C_P	
MGTREFCLK0N_221	AL10	FMC_HPC0_GBTCLK0_M2C_C_N[2]	D5	GBTCLK0_ M2C_N	
MGTREFCLK1P_221	AK13	FMC_HPC0_GBTCLK1_M2C_C_P[2]	B20	GBTCLK1_ M2C_P	
MGTREFCLK1N_221	AK12	FMC_HPC0_GBTCLK1_M2C_C_N[2]	B21	GBTCLK1_ M2C_N	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-28: **VCU110 FPGA U1 GTH Quad 222 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_222	AW7	FMC_HPC1_DP4_C2M_P	A34	DP4_C2M_P	FMC HPC1 J2
MGTHTXN0_222	AW6	FMC_HPC1_DP4_C2M_N	A35	DP4_C2M_N	
MGTHRXP0_222	AW2	FMC_HPC1_DP4_M2C_P	A14	DP4_M2C_P	
MGTHRXN0_222	AW1	FMC_HPC1_DP4_M2C_N	A15	DP4_M2C_N	
MGTHTXP1_222	AV9	FMC_HPC1_DP5_C2M_P	A38	DP5_C2M_P	
MGTHTXN1_222	AV8	FMC_HPC1_DP5_C2M_N	A39	DP5_C2M_N	
MGTHRXP1_222	AV4	FMC_HPC1_DP5_M2C_P	A18	DP5_M2C_P	
MGTHRXN1_222	AV3	FMC_HPC1_DP5_M2C_N	A19	DP5_M2C_N	
MGTHTXP2_222	AU7	FMC_HPC1_DP6_C2M_P	B36	DP6_C2M_P	
MGTHTXN2_222	AU6	FMC_HPC1_DP6_C2M_N	B37	DP6_C2M_N	
MGTHRXP2_222	AU2	FMC_HPC1_DP6_M2C_P	B16	DP6_M2C_P	
MGTHRXN2_222	AU1	FMC_HPC1_DP6_M2C_N	B17	DP6_M2C_N	
MGTHTXP3_222	AT9	FMC_HPC1_DP7_C2M_P	B32	DP7_C2M_P	
MGTHTXN3_222	AT8	FMC_HPC1_DP7_C2M_N	B33	DP7_C2M_N	
MGTHRXP3_222	AT4	FMC_HPC1_DP7_M2C_P	B12	DP7_M2C_P	
MGTHRXN3_222	AT3	FMC_HPC1_DP7_M2C_N	B13	DP7_M2C_N	
MGTREFCLK0P_222	AJ11	FMC_HPC1_GBTCLK0_M2C_P[2]	D4	GBTCLK0_ M2C_P	
MGTREFCLK0N_222	AJ10	FMC_HPC1_GBTCLK0_M2C_N[2]	D5	GBTCLK0_ M2C_N	
MGTREFCLK1P_222	AH13	FMC_HPC1_GBTCLK1_M2C_P[2]	B20	GBTCLK1_ M2C_P	
MGTREFCLK1N_222	AH12	FMC_HPC1_GBTCLK1_M2C_N[2]	B21	GBTCLK1_ M2C_N	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-29: **VCU110 FPGA U1 GTH Quad 224 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_224	AR7	FMC_HPC1_DP0_C2M_P	C2	DP0_C2M_P	FMC HPC1 J2
MGTHTXN0_224	AR6	FMC_HPC1_DP0_C2M_N	C3	DP0_C2M_N	
MGTHRXP0_224	AR2	FMC_HPC1_DP0_M2C_P	C6	DP0_M2C_P	
MGTHRXN0_224	AR1	FMC_HPC1_DP0_M2C_N	C7	DP0_M2C_N	
MGTHTXP1_224	AP9	FMC_HPC1_DP1_C2M_P	A22	DP1_C2M_P	
MGTHTXN1_224	AP8	FMC_HPC1_DP1_C2M_N	A23	DP1_C2M_N	
MGTHRXP1_224	AP4	FMC_HPC1_DP1_M2C_P	A2	DP1_M2C_P	
MGTHRXN1_224	AP3	FMC_HPC1_DP1_M2C_N	A3	DP1_M2C_N	
MGTHTXP2_224	AN7	FMC_HPC1_DP2_C2M_P	A26	DP2_C2M_P	
MGTHTXN2_224	AN6	FMC_HPC1_DP2_C2M_N	A27	DP2_C2M_N	
MGTHRXP2_224	AN2	FMC_HPC1_DP2_M2C_P	A6	DP2_M2C_P	
MGTHRXN2_224	AN1	FMC_HPC1_DP2_M2C_N	A7	DP2_M2C_N	
MGTHTXP3_224	AM9	FMC_HPC1_DP3_C2M_P	A30	DP3_C2M_P	
MGTHTXN3_224	AM8	FMC_HPC1_DP3_C2M_N	A31	DP3_C2M_N	
MGTHRXP3_224	AM4	FMC_HPC1_DP3_M2C_P	A10	DP3_M2C_P	
MGTHRXN3_224	AM3	FMC_HPC1_DP3_M2C_N	A11	DP3_M2C_N	
MGTREFCLK0P_224	AG11	FMC_HPC1_GBTCLK0_M2C_P[2]	D4	GBTCLK0_ M2C_P	
MGTREFCLK0N_224	AG10	FMC_HPC1_GBTCLK0_M2C_N[2]	D5	GBTCLK0_ M2C_N	
MGTREFCLK1P_224	AF13	FMC_HPC1_GBTCLK1_M2C_P[2]	B20	GBTCLK1_ M2C_P	
MGTREFCLK1N_224	AF12	FMC_HPC1_GBTCLK1_M2C_N[2]	B21	GBTCLK1_ M2C_N	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-30: **VCU110 FPGA U1 GTH Quad 225 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_225	AL7	HMC_L1TX_0_P	AD18	L1RXP_0	HMC U160
MGTHTXN0_225	AL6	HMC_L1TX_0_N	AD17	L1RXN_0	
MGTHRXP0_225	AL2	HMC_L1RX_0_C_P[2]	AF24	L1TXP_0	
MGTHRXN0_225	AL1	HMC_L1RX_0_C_N[2]	AF23	L1TXN_0	
MGTHTXP1_225	AK9	HMC_L1TX_2_P	AK16	L1RXP_2	
MGTHTXN1_225	AK8	HMC_L1TX_2_N	AK15	L1RXN_2	
MGTHRXP1_225	AK4	HMC_L1RX_2_C_P[2]	AG17	L1TXP_2	
MGTHRXN1_225	AK3	HMC_L1RX_2_C_N[2]	AG16	L1TXN_2	
MGTHTXP2_225	AJ7	HMC_L1TX_1_P	AE19	L1RXP_1	
MGTHTXN2_225	AJ6	HMC_L1TX_1_N	AE18	L1RXN_1	
MGTHRXP2_225	AJ2	HMC_L1RX_1_C_P[2]	AE23	L1TXP_1	
MGTHRXN2_225	AJ1	HMC_L1RX_1_C_N[2]	AE22	L1TXN_1	
MGTHTXP3_225	AH9	HMC_L1TX_6_P	AH22	L1RXP_6	
MGTHTXN3_225	AH8	HMC_L1TX_6_N	AH21	L1RXN_6	
MGTHRXP3_225	AH4	HMC_L1RX_6_C_P[2]	AK20	L1TXP_6	
MGTHRXN3_225	AH3	HMC_L1RX_6_C_N[2]	AK19	L1TXN_6	
MGTREFCLK0P_225	AE11	NA	NA	NA	NA
MGTREFCLK0N_225	AE10	NA	NA	NA	
MGTREFCLK1P_225	AD13	NA	NA	NA	
MGTREFCLK1N_225	AD12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-31: **VCU110 FPGA U1 GTH Quad 226 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_226	AG7	HMC_L1TX_4_P	AF20	L1RXP_4	HMC U160
MGTHTXN0_226	AG6	HMC_L1TX_4_N	AF19	L1RXN_4	
MGTHRXP0_226	AG2	HMC_L1RX_4_C_P[2]	AG25	L1TXP_4	
MGTHRXN0_226	AG1	HMC_L1RX_4_C_N[2]	AG24	L1TXN_4	
MGTHTXP1_226	AF9	HMC_L1TX_3_P	AK24	L1RXP_3	
MGTHTXN1_226	AF8	HMC_L1TX_3_N	AK23	L1RXN_3	
MGTHRXP1_226	AF4	HMC_L1RX_3_C_P[2]	AH18	L1TXP_3	
MGTHRXN1_226	AF3	HMC_L1RX_3_C_N[2]	AH17	L1TXN_3	
MGTHTXP2_226	AE7	HMC_L1TX_7_P	AJ23	L1RXP_7	
MGTHTXN2_226	AE6	HMC_L1TX_7_N	AJ22	L1RXN_7	
MGTHRXP2_226	AE2	HMC_L1RX_7_C_P[2]	AJ19	L1TXP_7	
MGTHRXN2_226	AE1	HMC_L1RX_7_C_N[2]	AJ18	L1TXN_7	
MGTHTXP3_226	AD9	HMC_L1TX_5_P	AG21	L1RXP_5	
MGTHTXN3_226	AD8	HMC_L1TX_5_N	AG20	L1RXN_5	
MGTHRXP3_226	AD4	HMC_L1RX_5_C_P[2]	AJ27	L1TXP_5	
MGTHRXN3_226	AD3	HMC_L1RX_5_C_N[2]	AJ26	L1TXN_5	
MGTREFCLK0P_226	AC11	HMC_SI5328_OUT2_BUF2_C_P[2]	35	CKOUT2_P	SI5328 U57
MGTREFCLK0N_226	AC10	HMC_SI5328_OUT2_BUF2_C_N[2]	34	CKOUT2_N	
MGTREFCLK1P_226	AB13	NA	NA	NA	NA
MGTREFCLK1N_226	AB12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-32: **VCU110 FPGA U1 GTH Quad 227 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_227	AC7	HMC_L1TX_11_P	AG29	L1RXP_11	HMC U160
MGTHTXN0_227	AC6	HMC_L1TX_11_N	AG28	L1RXN_11	
MGTHRXP0_227	AC2	HMC_L1RX_11_C_P[2]	AH26	L1TXP_11	
MGTHRXN0_227	AC1	HMC_L1RX_11_C_N[2]	AH25	L1TXN_11	
MGTHTXP1_227	AB9	HMC_L1TX_14_P	AE27	L1RXP_14	
MGTHTXN1_227	AB8	HMC_L1TX_14_N	AE26	L1RXN_14	
MGTHRXP1_227	AB4	HMC_L1RX_14_C_P[2]	AD30	L1TXP_14	
MGTHRXN1_227	AB3	HMC_L1RX_14_C_N[2]	AD29	L1TXN_14	
MGTHTXP2_227	AA7	HMC_L1TX_15_P	AF28	L1RXP_15	
MGTHTXN2_227	AA6	HMC_L1TX_15_N	AF27	L1RXN_15	
MGTHRXP2_227	AA2	HMC_L1RX_15_C_P[2]	AK28	L1TXP_15	
MGTHRXN2_227	AA1	HMC_L1RX_15_C_N[2]	AK27	L1TXN_15	
MGTHTXP3_227	Y9	HMC_L1TX_13_P	AD26	L1RXP_13	
MGTHTXN3_227	Y8	HMC_L1TX_13_N	AD25	L1RXN_13	
MGTHRXP3_227	Y4	HMC_L1RX_13_C_P[2]	AC29	L1TXP_13	
MGTHRXN3_227	Y3	HMC_L1RX_13_C_N[2]	AC28	L1TXN_13	
MGTREFCLK0P_227	AA11	NA	NA	NA	NA
MGTREFCLK0N_227	AA10	NA	NA	NA	
MGTREFCLK1P_227	Y13	NA	NA	NA	
MGTREFCLK1N_227	Y12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-33: **VCU110 FPGA U1 GTH Quad 228 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_228	W7	HMC_L1TX_12_P	AC25	L1RXP_12	HMC U160
MGTHTXN0_228	W6	HMC_L1TX_12_N	AC24	L1RXN_12	
MGTHRXP0_228	W2	HMC_L1RX_12_C_P[2]	AB28	L1TXP_12	
MGTHRXN0_228	W1	HMC_L1RX_12_C_N[2]	AB27	L1TXN_12	
MGTHTXP1_228	V9	HMC_L1TX_10_P	AH30	L1RXP_10	
MGTHTXN1_228	V8	HMC_L1TX_10_N	AH29	L1RXN_10	
MGTHRXP1_228	V4	HMC_L1RX_10_C_P[2]	AD22	L1TXP_10	
MGTHRXN1_228	V3	HMC_L1RX_10_C_N[2]	AD21	L1TXN_10	
MGTHTXP2_228	U7	HMC_L1TX_9_P	W28	L1RXP_9	
MGTHTXN2_228	U6	HMC_L1TX_9_N	W27	L1RXN_9	
MGTHRXP2_228	U2	HMC_L1RX_9_C_P[2]	Y26	L1TXP_9	
MGTHRXN2_228	U1	HMC_L1RX_9_C_N[2]	Y25	L1TXN_9	
MGTHTXP3_228	T9	HMC_L1TX_8_P	Y30	L1RXP_8	
MGTHTXN3_228	T8	HMC_L1TX_8_N	Y29	L1RXN_8	
MGTHRXP3_228	T4	HMC_L1RX_8_C_P[2]	AA27	L1TXP_8	
MGTHRXN3_228	T3	HMC_L1RX_8_C_N[2]	AA26	L1TXN_8	
MGTREFCLK0P_228	W11	NA	NA	NA	NA
MGTREFCLK0N_228	W10	NA	NA	NA	
MGTREFCLK1P_228	V13	NA	NA	NA	
MGTREFCLK1N_228	V12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-34: **VCU110 FPGA U1 GTH Quad 229 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_229	R7	HMC_L0TX_12_P	H25	L0RXP_12	HMC U160
MGTHTXN0_229	R6	HMC_L0TX_12_N	H24	L0RXN_12	
MGTHRXP0_229	R2	HMC_L0RX_12_C_P[2]	J28	L0TXP_12	
MGTHRXN0_229	R1	HMC_L0RX_12_C_N[2]	J27	L0TXN_12	
MGTHTXP1_229	P9	HMC_L0TX_9_P	M28	L0RXP_9	
MGTHTXN1_229	P8	HMC_L0TX_9_N	M27	L0RXN_9	
MGTHRXP1_229	P4	HMC_L0RX_9_C_P[2]	L26	L0TXP_9	
MGTHRXN1_229	P3	HMC_L0RX_9_C_N[2]	L25	L0TXN_9	
MGTHTXP2_229	N7	HMC_L0TX_13_P	G26	L0RXP_13	
MGTHTXN2_229	N6	HMC_L0TX_13_N	G25	L0RXN_13	
MGTHRXP2_229	N2	HMC_L0RX_13_C_P[2]	H29	L0TXP_13	
MGTHRXN2_229	N1	HMC_L0RX_13_C_N[2]	H28	L0TXN_13	
MGTHTXP3_229	M9	HMC_L0TX_8_P	L30	L0RXP_8	
MGTHTXN3_229	M8	HMC_L0TX_8_N	L29	L0RXN_8	
MGTHRXP3_229	M4	HMC_L0RX_8_C_P[2]	K27	L0TXP_8	
MGTHRXN3_229	M3	HMC_L0RX_8_C_N[2]	K26	L0TXN_8	
MGTREFCLK0P_229	U11	NA	NA	NA	NA
MGTREFCLK0N_229	U10	NA	NA	NA	
MGTREFCLK1P_229	T13	NA	NA	NA	
MGTREFCLK1N_229	T12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-35: **VCU110 FPGA U1 GTH Quad 230 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_230	L7	HMC_L0TX_10_P	C30	L0RXP_10	HMC U160
MGTHTXN0_230	L6	HMC_L0TX_10_N	C29	L0RXN_10	
MGTHRXP0_230	L2	HMC_L0RX_10_C_P[2]	G22	L0TXP_10	
MGTHRXN0_230	L1	HMC_L0RX_10_C_N[2]	G21	L0TXN_10	
MGTHTXP1_230	K9	HMC_L0TX_14_P	F27	L0RXP_14	
MGTHTXN1_230	K8	HMC_L0TX_14_N	F26	L0RXN_14	
MGTHRXP1_230	K4	HMC_L0RX_14_C_P[2]	G30	L0TXP_14	
MGTHRXN1_230	K3	HMC_L0RX_14_C_N[2]	G29	L0TXN_14	
MGTHTXP2_230	J7	HMC_L0TX_0_P	G18	L0RXP_0	
MGTHTXN2_230	J6	HMC_L0TX_0_N	G17	L0RXN_0	
MGTHRXP2_230	J2	HMC_L0RX_0_C_P[2]	E24	L0TXP_0	
MGTHRXN2_230	J1	HMC_L0RX_0_C_N[2]	E23	L0TXN_0	
MGTHTXP3_230	H9	HMC_L0TX_1_P	F19	L0RXP_1	
MGTHTXN3_230	H8	HMC_L0TX_1_N	F18	L0RXN_1	
MGTHRXP3_230	H4	HMC_L0RX_1_C_P[2]	F23	L0TXP_1	
MGTHRXN3_230	H3	HMC_L0RX_1_C_N[2]	F22	L0TXN_1	
MGTREFCLK0P_230	R11	HMC_SI5328_OUT2_BUF1_C_P[2]	35	CKOUT2_P	SI5328 U57
MGTREFCLK0N_230	R10	HMC_SI5328_OUT2_BUF1_C_N[2]	34	CKOUT2_N	
MGTREFCLK1P_230	P13	NA	NA	NA	NA
MGTREFCLK1N_230	P12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-36: **VCU110 FPGA U1 GTH Quad 231 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_231	G7	HMC_L0TX_4_P	E20	L0RXP_4	HMC U160
MGTHTXN0_231	G6	HMC_L0TX_4_N	E19	L0RXN_4	
MGTHRXP0_231	G2	HMC_L0RX_4_C_P[2]	D25	L0TXP_4	
MGTHRXN0_231	G1	HMC_L0RX_4_C_N[2]	D24	L0TXN_4	
MGTHTXP1_231	F9	HMC_L0TX_11_P	D29	L0RXP_11	
MGTHTXN1_231	F8	HMC_L0TX_11_N	D28	L0RXN_11	
MGTHRXP1_231	F4	HMC_L0RX_11_C_P[2]	C26	L0TXP_11	
MGTHRXN1_231	F3	HMC_L0RX_11_C_N[2]	C25	L0TXN_11	
MGTHTXP2_231	G11	HMC_L0TX_6_P	C22	L0RXP_6	
MGTHTXN2_231	G10	HMC_L0TX_6_N	C21	L0RXN_6	
MGTHRXP2_231	G16	HMC_L0RX_6_C_P[2]	A20	L0TXP_6	
MGTHRXN2_231	G15	HMC_L0RX_6_C_N[2]	A19	L0TXN_6	
MGTHTXP3_231	F13	HMC_L0TX_2_P	A16	L0RXP_2	
MGTHTXN3_231	F12	HMC_L0TX_2_N	A15	L0RXN_2	
MGTHRXP3_231	E16	HMC_L0RX_2_C_P[2]	D17	L0TXP_2	
MGTHRXN3_231	E15	HMC_L0RX_2_C_N[2]	D16	L0TXN_2	
MGTREFCLK0P_231	N11	NA	NA	NA	NA
MGTREFCLK0N_231	N10	NA	NA	NA	
MGTREFCLK1P_231	M13	NA	NA	NA	
MGTREFCLK1N_231	M12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-37: **VCU110 FPGA U1 GTH Quad 232 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_232	E7	HMC_L0TX_3_P	A24	L0RXP_3	HMC U160
MGTHTXN0_232	E6	HMC_L0TX_3_N	A23	L0RXN_3	
MGTHRXP0_232	E2	HMC_L0RX_3_C_P[2]	C18	L0TXP_3	
MGTHRXN0_232	E1	HMC_L0RX_3_C_N[2]	C17	L0TXN_3	
MGTHTXP1_232	E11	HMC_L0TX_15_P	E28	L0RXP_15	
MGTHTXN1_232	E10	HMC_L0TX_15_N	E27	L0RXN_15	
MGTHRXP1_232	D4	HMC_L0RX_15_C_P[2]	A28	L0TXP_15	
MGTHRXN1_232	D3	HMC_L0RX_15_C_N[2]	A27	L0TXN_15	
MGTHTXP2_232	C7	HMC_L0TX_5_P	D21	L0RXP_5	
MGTHTXN2_232	C6	HMC_L0TX_5_N	D20	L0RXN_5	
MGTHRXP2_232	C2	HMC_L0RX_5_C_P[2]	B27	L0TXP_5	
MGTHRXN2_232	C1	HMC_L0RX_5_C_N[2]	B26	L0TXN_5	
MGTHTXP3_232	A7	HMC_L0TX_7_P	B23	L0RXP_7	
MGTHTXN3_232	A6	HMC_L0TX_7_N	B22	L0RXN_7	
MGTHRXP3_232	B4	HMC_L0RX_7_C_P[2]	B19	L0TXP_7	
MGTHRXN3_232	B3	HMC_L0RX_7_C_N[2]	B18	L0TXN_7	
MGTREFCLK0P_232	L11	NA	NA	NA	NA
MGTREFCLK0N_232	L10	NA	NA	NA	
MGTREFCLK1P_232	K13	NA	NA	NA	
MGTREFCLK1N_232	K12	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-38: **VCU110 FPGA U1 GTH Quad 233 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_233	D9	PCIE_CABLE_TX3_C_P[2]	A11	PETP3	PCIe cable connector J136
MGTHTXN0_233	D8	PCIE_CABLE_TX3_C_N[2]	A12	PETN3	
MGTHRXP0_233	D14	PCIE_CABLE_RX3_P	B11	PERP3	
MGTHRXN0_233	D13	PCIE_CABLE_RX3_N	B12	PERN3	
MGTHTXP1_233	C11	PCIE_CABLE_TX2_C_P[2]	A8	PETP2	
MGTHTXN1_233	C10	PCIE_CABLE_TX2_C_N[2]	A9	PETN2	
MGTHRXP1_233	C16	PCIE_CABLE_RX2_P	B8	PERP2	
MGTHRXN1_233	C15	PCIE_CABLE_RX2_N	B9	PERN2	
MGTHTXP2_233	B9	PCIE_CABLE_TX1_C_P[2]	A5	PETP1	
MGTHTXN2_233	B8	PCIE_CABLE_TX1_C_N[2]	A6	PETN1	
MGTHRXP2_233	B14	PCIE_CABLE_RX1_P	B5	PERP1	
MGTHRXN2_233	B13	PCIE_CABLE_RX1_N	B6	PERN1	
MGTHTXP3_233	A11	PCIE_CABLE_TX0_C_P[2]	A2	PETP0	
MGTHTXN3_233	A10	PCIE_CABLE_TX0_C_N[2]	A3	PETN0	
MGTHRXP3_233	A16	PCIE_CABLE_RX0_P	B2	PERP0	
MGTHRXN3_233	A15	PCIE_CABLE_RX0_N	B3	PERN0	
MGTREFCLK0P_233	J11	PCIE_CABLE_CLK_C_P[2]	A14	CREFCLKP	
MGTREFCLK0N_233	J10	PCIE_CABLE_CLK_C_N[2]	A15	CREFCLKN	
MGTREFCLK1P_233	H13	NA	NA	NA	NA
MGTREFCLK1N_233	H12	NA	NA	NA	

Notes:
1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

For additional information on GTH transceivers, see *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 7].

Also see *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182) [Ref 6].

PCI Express Endpoint Connectivity

[Figure 1-2, callout 16]

The 4-lane PCI Express cable connector J136 performs data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications and 8.0 GT/s for Gen3 applications. The PCIe transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair.

The PCIe clock is input from the J136 PCIe cable connector and is AC coupled to FPGA U1 REFCLK0 pins of GTH Quad 233.

The PCIe J136 connection to FPGA U1 GTH Quad 233 is detailed in Table 1-39.

Table 1-39: **VCU110 PCIe Cable Connector J136 to FPGA U1 GTH Quad 233 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name(1)	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_233	D9	PCIE_CABLE_TX3_C_P(2)	A11	PETP3	PCIe cable connector J136
MGTHTXN0_233	D8	PCIE_CABLE_TX3_C_N(2)	A12	PETN3	
MGTHRXP0_233	D14	PCIE_CABLE_RX3_P	B11	PERP3	
MGTHRXN0_233	D13	PCIE_CABLE_RX3_N	B12	PERN3	
MGTHTXP1_233	C11	PCIE_CABLE_TX2_C_P(2)	A8	PETP2	
MGTHTXN1_233	C10	PCIE_CABLE_TX2_C_N(2)	A9	PETN2	
MGTHRXP1_233	C16	PCIE_CABLE_RX2_P	B8	PERP2	
MGTHRXN1_233	C15	PCIE_CABLE_RX2_N	B9	PERN2	
MGTHTXP2_233	B9	PCIE_CABLE_TX1_C_P(2)	A5	PETP1	
MGTHTXN2_233	B8	PCIE_CABLE_TX1_C_N(2)	A6	PETN1	
MGTHRXP2_233	B14	PCIE_CABLE_RX1_P	B5	PERP1	
MGTHRXN2_233	B13	PCIE_CABLE_RX1_N	B6	PERN1	
MGTHTXP3_233	A11	PCIE_CABLE_TX0_C_P(2)	A2	PETP0	
MGTHTXN3_233	A10	PCIE_CABLE_TX0_C_N(2)	A3	PETN0	
MGTHRXP3_233	A16	PCIE_CABLE_RX0_P	B2	PERP0	
MGTHRXN3_233	A15	PCIE_CABLE_RX0_N	B3	PERN0	
MGTREFCLK0P_233	J11	PCIE_CABLE_CLK_C_P(2)	A14	CREFCLKP	
MGTREFCLK0N_233	J10	PCIE_CABLE_CLK_C_N(2)	A15	CREFCLKN	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

For additional information about UltraScale PCIe functionality, see *UltraScale Devices Gen 3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156) [Ref 8]. Additional information about the PCI Express standard is available [Ref 26].

CFP Module Quad Connectors (CFP4)

[Figure 1-2, callout 17]

The VCU110 board contains a 100G C form-factor pluggable (CFP) Quad connector assembly comprised of four sub-module assemblies (J107-J110), each of which accepts a CFP optical module. The connector is housed within a single CFP4 cage assembly.

Figure 1-14 shows a typical CFP module connector circuitry instantiation.

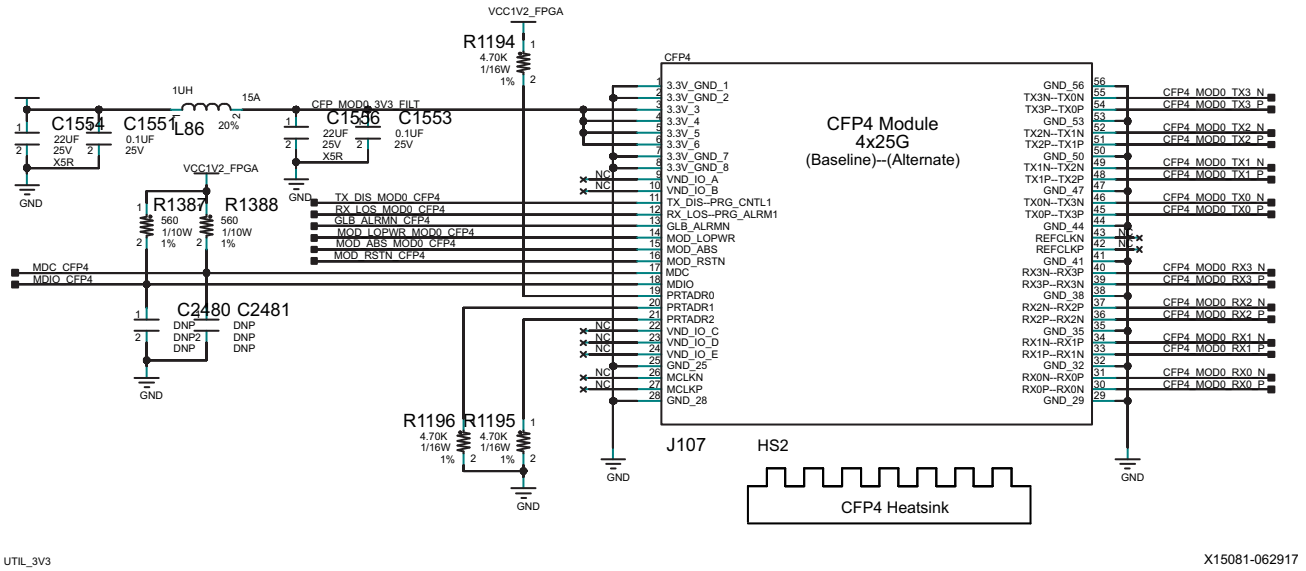

Figure 1-14: **CFP Module Connector Circuit**

The CFP module J107-J110 connections to the GTY Quads 122, 125, 127 and 128 are detailed in Table 1-40 through Table 1-42.

Table 1-40: **VCU110 FPGA U1 GTY Quad 122 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_122	AW40	CFP4_MOD0_TX3_P	54	TX3P--TX0P	CFP4 MOD0 J107
MGTYTXN0_122	AW41	CFP4_MOD0_TX3_N	55	TX3N--TX0N	
MGTYRXP0_122	AW45	CFP4_MOD0_RX3_P	39	RX3P--RX3N	
MGTYRXN0_122	AW46	CFP4_MOD0_RX3_N	40	RX3N--RX3P	
MGTYTXP1_122	AV38	CFP4_MOD0_TX2_P	51	TX2P--TX1P	
MGTYTXN1_122	AV39	CFP4_MOD0_TX2_N	52	TX2N--TX1N	
MGTYRXP1_122	AV43	CFP4_MOD0_RX2_P	36	RX2P--RX2N	
MGTYRXN1_122	AV44	CFP4_MOD0_RX2_N	37	RX2N--RX2P	
MGTYTXP2_122	AU40	CFP4_MOD0_TX1_P	48	TX1P--TX2P	
MGTYTXN2_122	AU41	CFP4_MOD0_TX1_N	49	TX1N--TX2N	
MGTYRXP2_122	AU45	CFP4_MOD0_RX1_P	33	RX1P--RX1N	
MGTYRXN2_122	AU46	CFP4_MOD0_RX1_N	34	RX1N--RX1P	
MGTYTXP3_122	AT38	CFP4_MOD0_TX0_P	45	TX0P--TX3P	
MGTYTXN3_122	AT39	CFP4_MOD0_TX0_N	46	TX0N--TX3N	
MGTYRXP3_122	AT43	CFP4_MOD0_RX0_P	30	RX0N--RX0P	
MGTYRXN3_122	AT44	CFP4_MOD0_RX0_N	31	RX0P--RX0N	

Table 1-40: **VCU110 FPGA U1 GTY Quad 122 Connections *(Cont'd)***

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTREFCLK0P_122	AJ36	CFP4_SI5328_OUT1_BUF1_C_P[2]	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_122	AJ37	CFP4_SI5328_OUT1_BUF1_C_N[2]	29	CKOUT1_N	
MGTREFCLK1P_122	AH34	NA	NA	NA	NA
MGTREFCLK1N_122	AH35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-41: **VCU110 FPGA U1 GTY Quad 125 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_125	W40	CFP4_MOD1_TX3_P	54	TX3P--TX0P	CFP4 MOD1 J108
MGTYTXN0_125	W41	CFP4_MOD1_TX3_N	55	TX3N--TX0N	
MGTYRXP0_125	W45	CFP4_MOD1_RX3_P	39	RX3P--RX3N	
MGTYRXN0_125	W46	CFP4_MOD1_RX3_N	40	RX3N--RX3P	
MGTYTXP1_125	V38	CFP4_MOD1_TX2_P	51	TX2P--TX1P	
MGTYTXN1_125	V39	CFP4_MOD1_TX2_N	52	TX2N--TX1N	
MGTYRXP1_125	V43	CFP4_MOD1_RX2_P	36	RX2P--RX2N	
MGTYRXN1_125	V44	CFP4_MOD1_RX2_N	37	RX2N--RX2P	
MGTYTXP2_125	U40	CFP4_MOD1_TX1_P	48	TX1P--TX2P	
MGTYTXN2_125	U41	CFP4_MOD1_TX1_N	49	TX1N--TX2N	
MGTYRXP2_125	U45	CFP4_MOD1_RX1_P	33	RX1P--RX1N	
MGTYRXN2_125	U46	CFP4_MOD1_RX1_N	34	RX1N--RX1P	
MGTYTXP3_125	T38	CFP4_MOD1_TX0_P	45	TX0P--TX3P	
MGTYTXN3_125	T39	CFP4_MOD1_TX0_N	46	TX0N--TX3N	
MGTYRXP3_125	T43	CFP4_MOD1_RX0_P	30	RX0N--RX0P	
MGTYRXN3_125	T44	CFP4_MOD1_RX0_N	31	RX0P--RX0N	
MGTREFCLK0P_125	W36	CFP4_SI5328_OUT1_BUF2_C_P[2]	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_125	W37	CFP4_SI5328_OUT1_BUF2_C_N[2]	29	CKOUT1_N	
MGTREFCLK1P_125	V34	NA	NA	NA	NA
MGTREFCLK1N_125	V35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-42: **VCU110 FPGA U1 GTY Quad 127 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name (1)	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_127	R40	CFP4_MOD2_TX3_P	54	TX3P--TX0P	CFP4 MOD2 J109
MGTYTXN0_127	R41	CFP4_MOD2_TX3_N	55	TX3N--TX0N	
MGTYRXP0_127	R45	CFP4_MOD2_RX3_P	39	RX3P--RX3N	
MGTYRXN0_127	R46	CFP4_MOD2_RX3_N	40	RX3N--RX3P	
MGTYTXP1_127	P38	CFP4_MOD2_TX2_P	51	TX2P--TX1P	
MGTYTXN1_127	P39	CFP4_MOD2_TX2_N	52	TX2N--TX1N	
MGTYRXP1_127	P43	CFP4_MOD2_RX2_P	36	RX2P--RX2N	
MGTYRXN1_127	P44	CFP4_MOD2_RX2_N	37	RX2N--RX2P	
MGTYTXP2_127	N40	CFP4_MOD2_TX1_P	48	TX1P--TX2P	
MGTYTXN2_127	N41	CFP4_MOD2_TX1_N	49	TX1N--TX2N	
MGTYRXP2_127	N45	CFP4_MOD2_RX1_P	33	RX1P--RX1N	
MGTYRXN2_127_	N46	CFP4_MOD2_RX1_N	34	RX1N--RX1P	
MGTYTXP3_127	M38	CFP4_MOD2_TX0_P	45	TX0P--TX3P	
MGTYTXN3_127	M39	CFP4_MOD2_TX0_N	46	TX0N--TX3N	
MGTYRXP3_127	M43	CFP4_MOD2_RX0_P	30	RX0N--RX0P	
MGTYRXN3_127	M44	CFP4_MOD2_RX0_N	31	RX0P--RX0N	
MGTREFCLK0P_127	U36	CFP4_SI5328_OUT1_BUF3_C_P(2)	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_127	U37	CFP4_SI5328_OUT1_BUF3_C_N(2)	29	CKOUT1_N	
MGTREFCLK1P_127	T34	NA	NA	NA	NA
MGTREFCLK1N_127	T35	NA	NA	NA	

Notes:

1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Table 1-43: **VCU110 FPGA U1 GTY Quad 128 Connections**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTYTXP0_128	E40	CFP4_MOD3_TX3_P	54	TX3P--TX0P	CFP4 MOD3 J110
MGTYTXN0_128	E41	CFP4_MOD3_TX3_N	55	TX3N--TX0N	
MGTYRXP0_128	E45	CFP4_MOD3_RX3_P	39	RX3P--RX3N	
MGTYRXN0_128	E46	CFP4_MOD3_RX3_N	40	RX3N--RX3P	
MGTYTXP1_128	E36	CFP4_MOD3_TX2_P	51	TX2P--TX1P	
MGTYTXN1_128	E37	CFP4_MOD3_TX2_N	52	TX2N--TX1N	
MGTYRXP1_128	D43	CFP4_MOD3_RX2_P	36	RX2P--RX2N	
MGTYRXN1_128	D44	CFP4_MOD3_RX2_N	37	RX2N--RX2P	
MGTYTXP2_128	C40	CFP4_MOD3_TX1_P	48	TX1P--TX2P	
MGTYTXN2_128	C41	CFP4_MOD3_TX1_N	49	TX1N--TX2N	
MGTYRXP2_128	C45	CFP4_MOD3_RX1_P	33	RX1P--RX1N	
MGTYRXN2_128	C46	CFP4_MOD3_RX1_N	34	RX1N--RX1P	
MGTYTXP3_128	A40	CFP4_MOD3_TX0_P	45	TX0P--TX3P	
MGTYTXN3_128	A41	CFP4_MOD3_TX0_N	46	TX0N--TX3N	
MGTYRXP3_128	B43	CFP4_MOD3_RX0_P	30	RX0N--RX0P	
MGTYRXN3_128	B44	CFP4_MOD3_RX0_N	31	RX0P--RX0N	
MGTREFCLK0P_128	L36	CFP4_SI5328_OUT1_BUF4_C_P[2]	28	CKOUT1_P	SI5328 U179
MGTREFCLK0N_128	L37	CFP4_SI5328_OUT1_BUF4_C_N[2]	29	CKOUT1_N	
MGTREFCLK1P_128	K34	CFP4_REC_CLOCK2_C_P(1)	12	CKIN2_P	SI5328 U179
MGTREFCLK1N_128	K35	CFP4_REC_CLOCK2_C_N(1)	13	CKIN2_N	

Notes:
1. MGT connections I/O standard not applicable
2. Series capacitor coupled

For additional information about the 100 Gb/s C form-factor pluggable module, see the *CFP MSA CFP4 Hardware Specification* [Ref 28].

10/100/1,000Mb/s Tri-Speed Ethernet PHY

[Figure 1-2, callout 18]

The VCU110 evaluation board uses the Marvell Alaska PHY device (88E1111) at U58 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1,000 Mb/s. The board supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through RJ-45 connector P3, a Halo HFJ11-1G01E-L12RL with built-in magnetics and status LEDs.

On power-up, or on reset, the PHY is configured to operate in SGMII mode with PHY address `0b00111` using the settings shown in Table 1-44. These settings can be over written using software commands passed over the MDIO interface.

Table 1-44: **Board Connections for PHY Configuration Pins**

Pin	Bit[2]	Bit[1]	Bit[0]		Description	Pin to Constant Mapping	
						Pin	Bit[2:0]
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr 00111. Do not advertise the PAUSE bit.	VCC2V5	111
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000		LED_LINK10	110
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.	LED_LINK100	101
CFG3	ANEG[0]	ENA_XC	DIS_125	111		LED_LINK1000	100
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	100	SGMII to Cu mode. Fiber/copper auto-detect disabled. Sleep move disabled.	LED_DUPLEX	011
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	110		LED_RX	010
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active-Low interrupt. 50Ω SerDes option.	LED_TX	001
						GND	000

Table 1-45 details the FPGA U1 to U58 M88E111 Ethernet PHY connections.

Table 1-45: FPGA U1 to Ethernet PHY U58 Connections

FPGA (U1) Pin	Net Name	I/O Standard	M88E111 PHY U58	
			Pin	Name
BB21	PHY_MDIO	LVCMOS18	M1	MDIO_SDA
BC18	PHY_MDC	LVCMOS18	L3	MDC_SCL
BC21	PHY_INT	LVCMOS18	L1	INT_B
BB18	PHY_RESET	LVCMOS18	K3	RESET_B

Notes:
1. Ethernet PHY U58 signals are level-shifted (U45) to 1.8V for interface to FPGA U1 bank 84.

Ethernet PHY Status LEDs

[Figure 1-2, callout 19]

The Ethernet PHY status LEDs are integrated into the metal frame of the P3 RJ-45 connector. These LEDs are visible on the left edge of the VCU110 board when it is installed into a PCIe

slot in a PC chassis. The two PHY status LEDs are integrated within the frame of the RJ45 Ethernet jack, as shown in Figure 1-15.

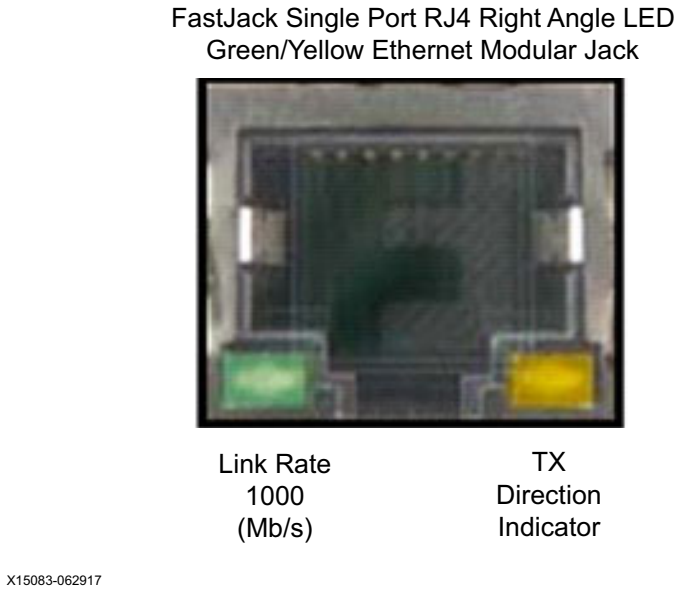

Figure 1-15: **Ethernet PHY Status LEDs**

Details about the Tri-Mode Ethernet MAC core are provided in *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)[Ref 9].

The product brief for the Marvell 88E1111 Alaska Gigabit Ethernet Transceiver can be found at the Marvell website [Ref 29]. The data sheet can be obtained under NDA with Marvell. Contact information is at the Marvell website [Ref 29].

Dual USB-to-UART Bridge

[Figure 1-2, callout 20]

The VCU110 evaluation board contains a Silicon Labs CP2105GM dual USB-to-UART bridge device (U34) which allows a connection to a host computer with a USB port. The USB cable is supplied in the VCU110 Evaluation Kit (standard type-A end to host computer, type micro-B end to VCU110 evaluation board connector J4). The CP2105GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the VCU110 evaluation board.

The dual UART interface connections are split between two components:

- UART1 SCI 4-wire interface is connected to the XCVU190 U1 FPGA
- UART2 ECI 2-wire interface is connected to the XC7Z010 U111 Zynq SoC system controller

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2105GM dual USB-to-UART bridge to appear as a pair of COM ports to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the VCU110 evaluation board. The driver assigns the lower PC COM port number to UART2 and the higher PC COM port number to UART1.

Table 1-46 lists the dual-UART U34 connections to FPGA U1 and system controller U111.

Table 1-46: **FPGA U1 to CP2105GM U34 Connections**

FPGA U1 Pin	Function	Direction	I/O Standard	Schematic Net Name	CP2105GM Device (U34)		
					Pin	Function	Direction
AR20	Receive	Input	LVCMOS18	USB_UART_TX	21	Transmit data	Output
AT20	Transmit	Output	LVCMOS18	USB_UART_RX	20	Receive data	Input
AR19	Clear to send	Output	LVCMOS18	USB_UART_CTS	18	Clear to send	Input
AU19	Request to send	Input	LVCMOS18	USB_UART_RTS	19	Request to send	Output

For more technical information on the CP2105GM and the VCP drivers, visit the Silicon Labs website [Ref 25].

Implement FPGA logic-based UART IP by using IP like the AXI UART Lite LogiCORE IP documented in the *AXI UART Lite LogiCORE IP Product Guide* (PG142) [Ref 10].

I2C Bus, Topology and Bus Switches

[Figure 1-2, callouts 21, 22]

The VCU110 evaluation board implements a 2-to-1 I2C bus arrangement. A single I2C bus from each of the FPGA U1 XCVU190 (IIC_MAIN_SCL/SDA_LS) and system controller Zynq SoC U111 (SYSCTLR_I2C_SCL/SDA) are wired to the same I2C bus through level-shifters (FPGA U1 is wired through level-shifter U77 and system controller U111 is wired through level-shifter U108). The output sides of U77 and U108 are wired in parallel to a common I2C bus (IIC_SDA and _SCL_MAIN). This common I2C bus is then routed to a pair of bus switches, a TI TCA9548 1-to-8 channel I2C bus switch (U28) and a TI PCA9544 1-to-4 channel I2C bus switch (U80). The bus switches can operate at speeds up to 400 kHz.

The VCU110 evaluation board I2C bus topology overview is shown in Figure 1-16.

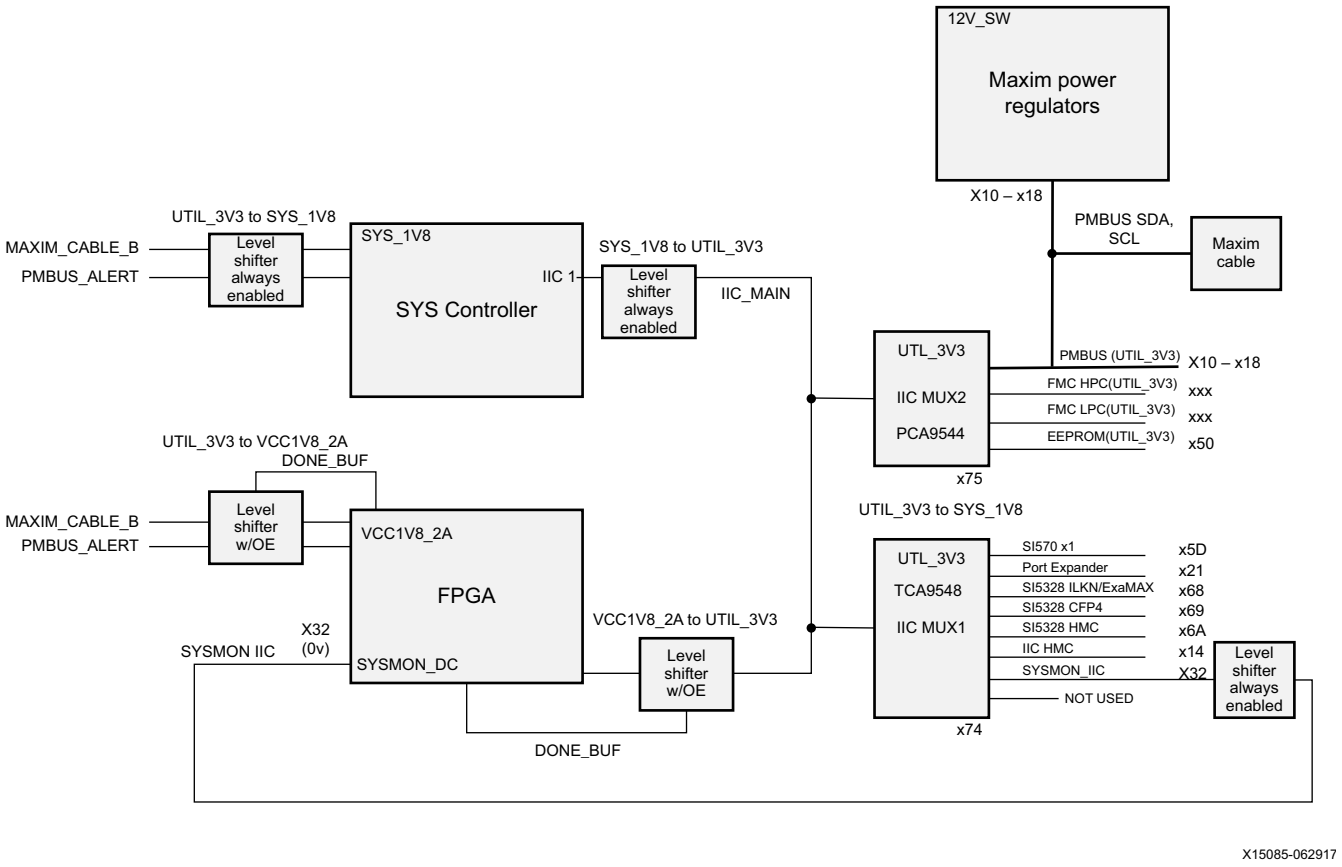

Figure 1-16: **I2C Bus Topology Overview**

IMPORTANT: *The TCA9548 U28 RESET_B pin 3 is connected to FPGA U1 bank 65 pin AR18 via level-shifter U44. The PCA9544 does not have a reset pin. FPGA pin AR18 LVCMOS18 net IIC_MUX_RESET_B_LS must be driven High to enable I2C bus transactions with the devices connected to U28.*

A zoomed in view of the I2C bus switches is shown in Figure 1-17.

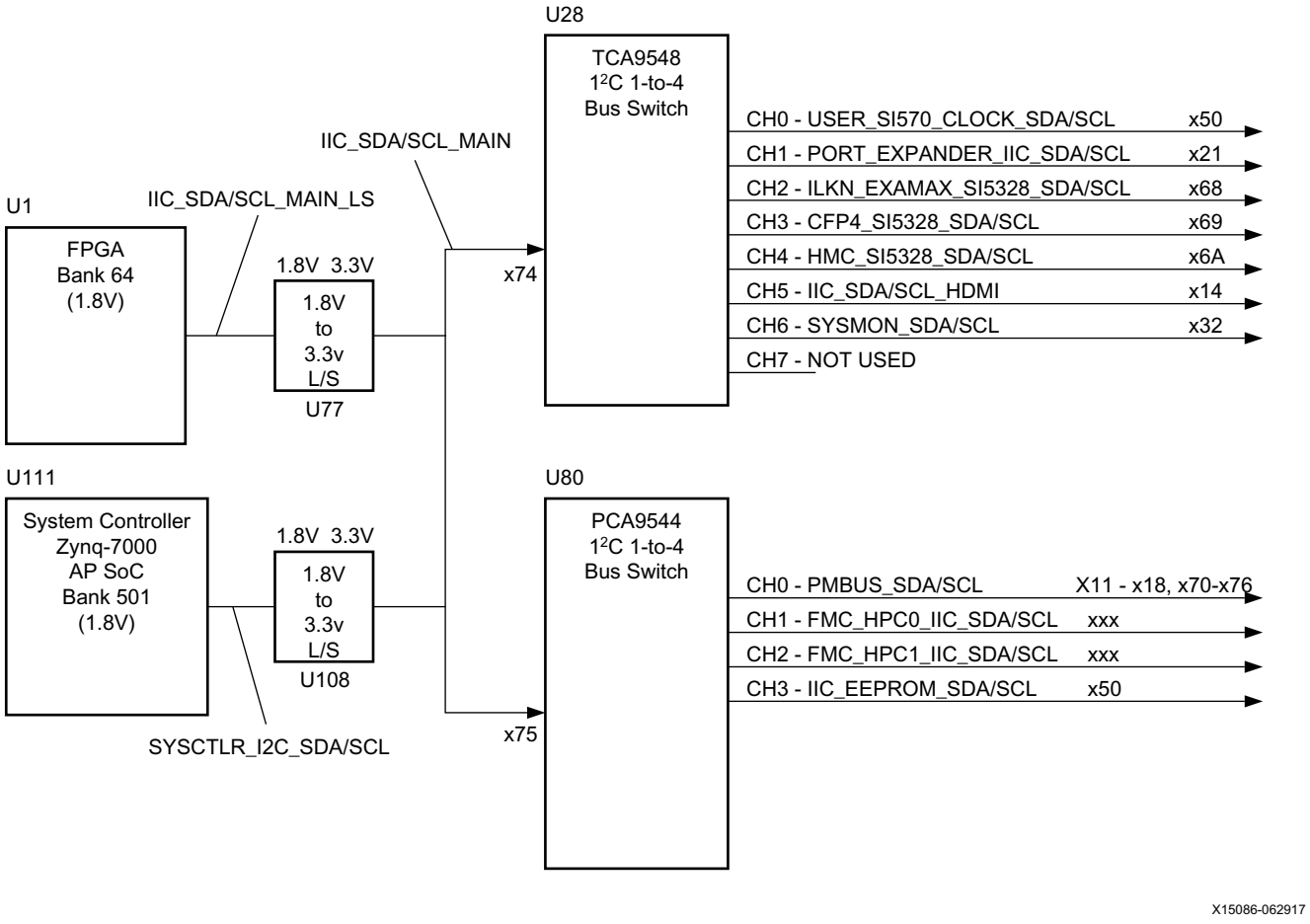

Figure 1-17: **I2C Bus IIC_MAIN Bus Switches**

User applications that communicate with devices on one of the downstream I2C buses must first set up a path to the desired bus through the U28 or U80 bus switch at I2C address `0x74` (`0b1110100`) or `0x75` (`0b1110101`) respectively. Table 1-47 lists the address for each bus.

Table 1-47: **I2C Devices**

I2C Device	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
TCA9548 8-channel bus switch	NA	0b1110100	0x74	U28 PCA9548
Si570 clock	0	0b1011101	0x5D	U32 SI570
I2C Port expander	1	0b0100001	0x21	U89 TCA6416
Ilkn. ExaMax Si5328 clock	2	0b1010000	0x50	U181 SI5328C
CFP4 Si5328 clock	3	0b1101001	0x69	U179 SI5328C

Table 1-47: **I2C Devices *(Cont'd)***

I2C Device	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
HMC Si5328 clock	4	0b1101010	0x6A	U57 SI5328B
HMC I2C	5	0b0010100	0x14	U160 HMC
FPGA SYSMON I2	6	0b0110010	0x32	U1 BANK 65
PCA9544 4-channel bus switch	NA	0b1110101	0x75	U80 PCA9544
PMBus regulators	0	0b0010000-0b0011000 0b1110000-0b1110110	0x10-x18 0x70-x76	MAXIM VREGs(1)
FMC HPC0 I2C	1	0bXXXXX00	0xXX	J22 FMC HPC
FMC HPC1 I2C	2	0bXXXXX00	0xXX	J2 FMC LPC
I2C EEPROM	3	0b1010000	0x50	U12 M24C08

Notes:

1. MAX15301: U4, U9, U30, U150, U156, U187; VT7701M: U166, U174, U175, U191, U192, U193 (See Table 1-66 for details).

Information about the TCA9548 and PCA9544 is available on the Texas Instruments Semiconductor website at [Ref 31].

For additional information on the Zynq-7000 SoC device I2C controller, see *Zynq-7000 SoC Data Sheet: Overview* (DS190) [Ref 11] and *Zynq-7000 SoC Technical Reference Manual* (UG585) [Ref 12].

Status and User LEDs

[Figure 1-2, callout 23]

Table 1-48 defines VCU110 board status and user LEDs.

Table 1-48: **VCU110 Board Status and User LEDs**

Reference Designator	Description
DS2	INIT
DS3	OR'D POWER GOOD
DS6	GPIO_LED_1
DS7	GPIO_LED_0
DS8	GPIO_LED_2
DS9	GPIO_LED_3
DS10	GPIO_LED_4
DS14	UTIL_3V3_PGOOD
DS15	MGTAVCC_PGOOD

Table 1-48: **VCU110 Board Status and User LEDs *(Cont'd)***

Reference Designator	Description
DS16	VCC1V2_PGOOD
DS17	MGTAVTT_PGOOD
DS19	VADJ_1V8_PGOOD
DS21	VCCINT_PGOOD
DS24	VCC1V8_PGOOD
DS25	MGTVCCAUX_PGOOD
DS26	12V ON
DS27	SYS_2V5 ON
DS28	SYS_1V8 ON
DS31	GPIO_LED_7
DS32	GPIO_LED_6
DS33	GPIO_LED_5
DS34	DONE
DS40	SYS_5VO ON
DS42	SYSCTLR INIT
DS43	SYSCTLR STATUS
DS44	SYSCTLR DONE
DS45	SYSCTLR ERROR
DS46	SYS_1VO ON
DS47	DDR4 C2 VTT ON
DS48	RLD3 VTT ON
DS49	QDR2+ VTT ON
DS52	UTIL_1V35_PGOOD
DS53	UTIL_0V9_PGOOD
DS54	VCC1V5_PGOOD
DS55	HMC1V2_PGOOD
EPHY P3 GREEN LED	ENET PHY LINK1000
EPHY P3 YELLOW LED	ENET PHY TX

User I/O

[Figure 1-2, callouts 23-26]

The VCU110 board provides the following user and general purpose I/O capabilities:

- Eight user LEDs (callout 23)
  - GPIO_LED [7-0]: DS31, DS32, DS33, DS10, DS9, DS8, DS6, DS7
- Five user pushbuttons and CPU reset switch (callout 24)
  - GPIO_SW [NESWC]: SW10, SW9, SW8, SW6, SW7
  - CPU_RESET: SW5 (callout 25)
- 4-position user DIP switch (callout 26)
  - GPIO_DIP_SW [3:0]: SW12

User GPIO LEDs

[Figure 1-2, callout 23]

Figure 1-18 shows the GPIO LED circuit.

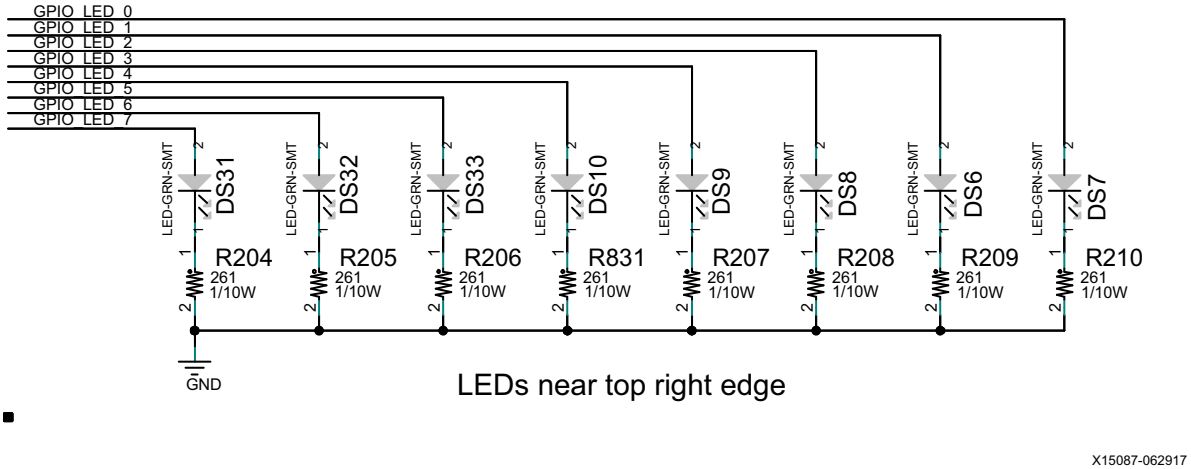

Figure 1-18: **User LEDs**

User Pushbuttons

[Figure 1-2, callout 24]

Figure 1-19 shows the user pushbuttons circuit.

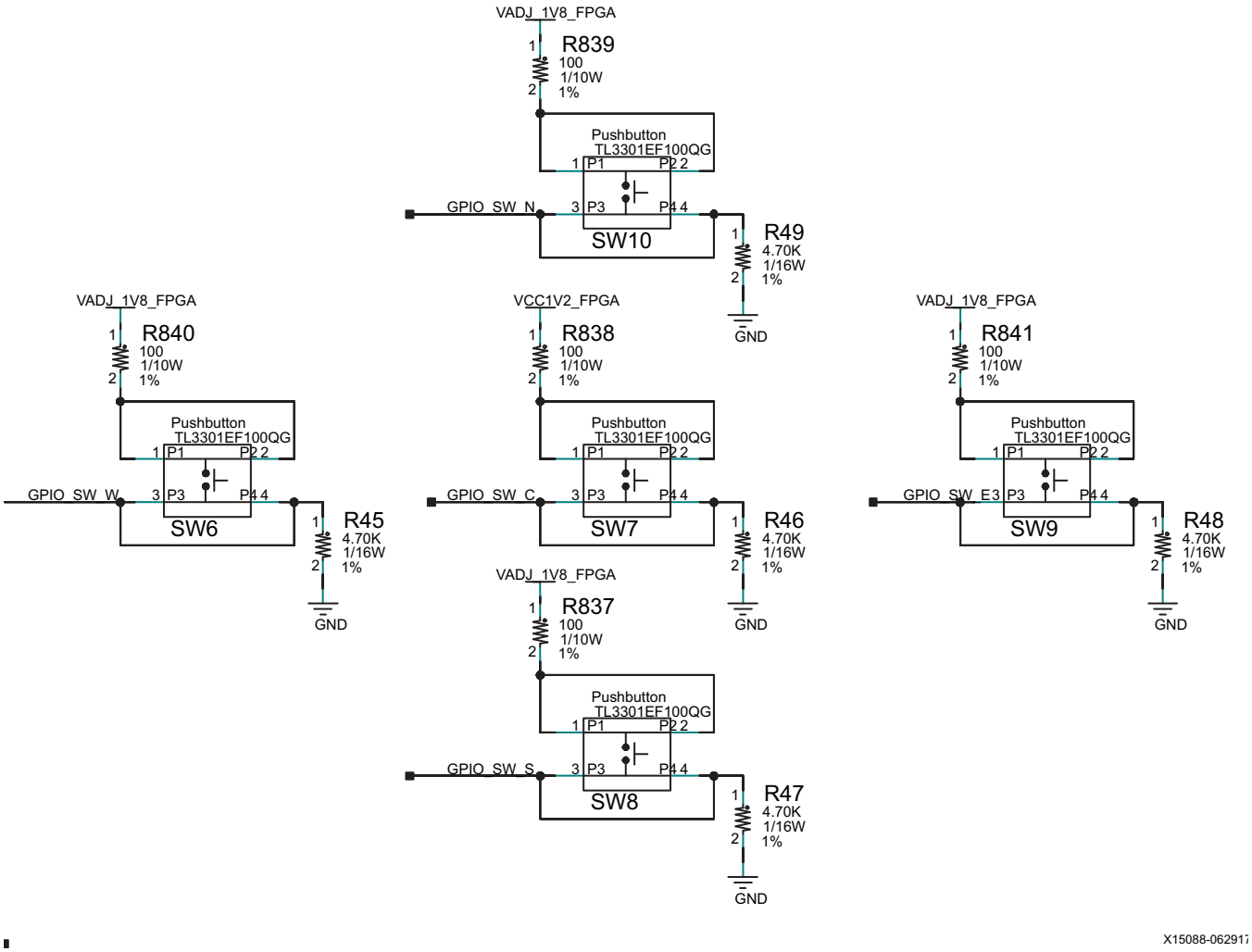

Figure 1-19: **User Pushbuttons**

CPU Reset Pushbutton

[Figure 1-2, callout 25]

Figure 1-20 shows the CPU reset pushbutton circuit.

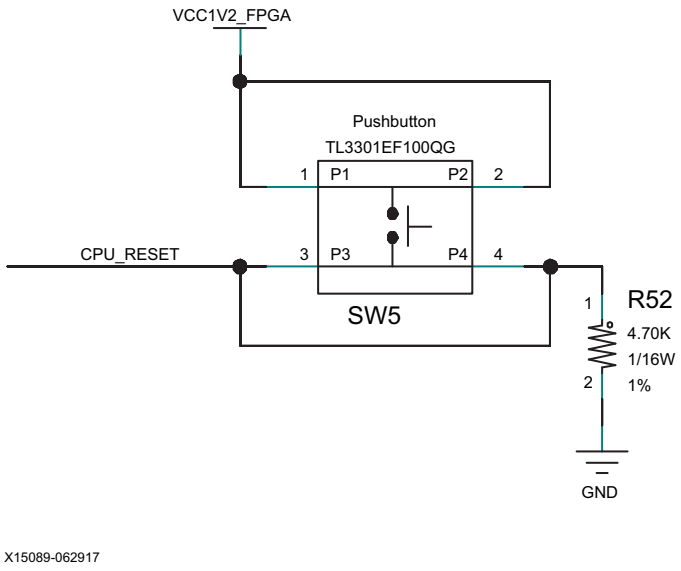

Figure 1-20: **CPU Reset Pushbutton**

GPIO DIP Switch

[Figure 1-2, callout 26]

Figure 1-21 shows the GPIO DIP switch circuit.

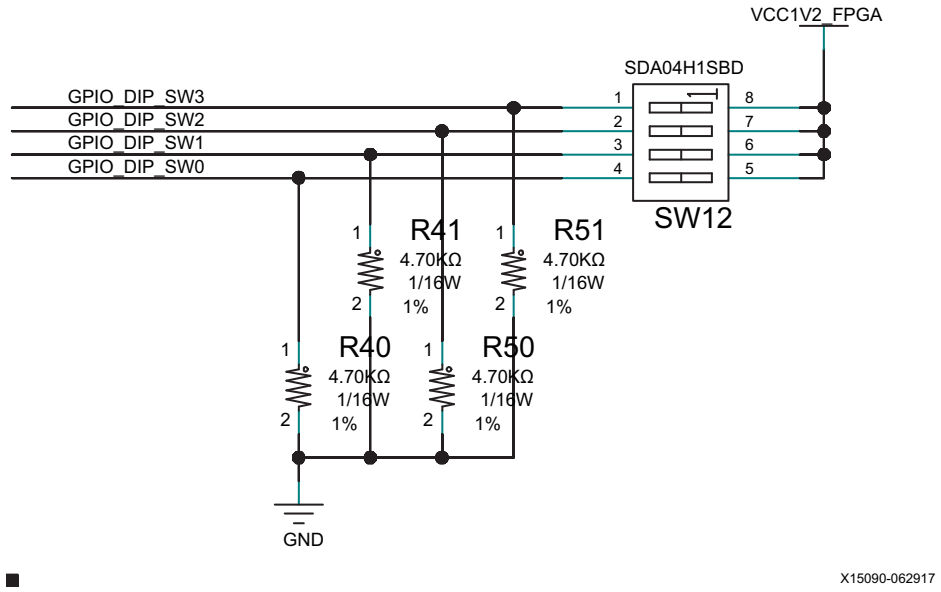

Figure 1-21: **CPU GPIO DIP Switch**

Table 1-49 lists the GPIO connections to FPGA U1.

Table 1-49: **VCU110 GPIO Connections to FPGA U1**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	GPIO
GPIO LEDs (Active-High)(1)			
N25	GPIO_LED_0	LVCMOS12	DS7.1
N22	GPIO_LED_1	LVCMOS12	DS6.1
M22	GPIO_LED_2	LVCMOS12	DS8.1
M26	GPIO_LED_3	LVCMOS12	DS9.1
M25	GPIO_LED_4	LVCMOS12	DS10.1
P24	GPIO_LED_5	LVCMOS12	DS33.1
N24	GPIO_LED_6	LVCMOS12	DS32.1
N23	GPIO_LED_7	LVCMOS12	DS31.1
Directional Pushbuttons (Active-High)			
AT11	GPIO_SW_N	LVCMOS18	SW10.3
AY13	GPIO_SW_E	LVCMOS18	SW9.3
AM16	GPIO_SW_W	LVCMOS18	SW6.3
BC16	GPIO_SW_S	LVCMOS18	SW8.3

Table 1-49: **VCU110 GPIO Connections to FPGA U1 *(Cont'd)***

FPGA Pin (U1)	Schematic Net Name	I/O Standard	GPIO
L26	GPIO_SW_C(2)	LVCMOS18	SW7.3
4-Pole DIP Switch (Active-High)			
BD28	GPIO_DIP_SW0	LVCMOS12	SW12.4
BC28	GPIO_DIP_SW1	LVCMOS12	SW12.3
BE26	GPIO_DIP_SW2	LVCMOS12	SW12.2
BF25	GPIO_DIP_SW3	LVCMOS12	SW12.1

Notes:

1. LED signals are level-shifted from 3.3V to 1.2V with SN74AVC4T245 drivers U47 and U49.
2. Pushbutton SW7 is level-shifted from 1.2V to 1.8V with SN74AVCT245 driver U197 for the U111 bank 501 connection.

User PMOD GPIO Header

[Figure 1-2, callout 29]

The VCU110 evaluation board supports one right-angle (FEMALE) PMOD GPIO receptacle J52. The PMOD nets connected to J52 are accessed through level-shifter U41 (PMOD0). The level-shifter is wired to XCVU190 FPGA U1 bank71.

Figure 1-22 shows the female GPIO PMOD header J52.

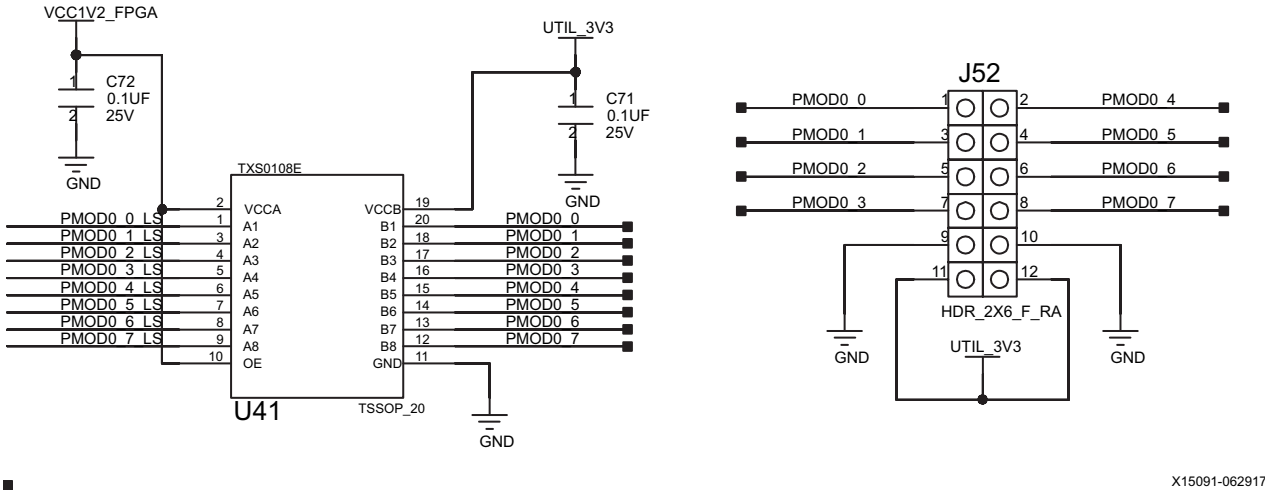

Figure 1-22: **PMOD Connectors J52 with Level-Shifter U41**

Table 1-50 shows the level-shifter U41 connections to FPGA U1.

Table 1-50: **PMOD Female J52 Connections through Level-Shifter U41 to FPGA U1**

XCVU190 (U1) Pin	Schematic Net Name	I/O Standard	Level-Shifter (U41)		Schematic Net Name	PMOD Connector Pin
			Side A 1.2V	Side B 3.3V		
L23	PMOD0_0_LS	LVCMOS12	U41.1	U41.20	PMOD0_0	J52.1
J22	PMOD0_1_LS	LVCMOS12	U41.3	U41.18	PMOD0_1	J52.3
J21	PMOD0_2_LS	LVCMOS12	U41.4	U41.17	PMOD0_2	J52.5
J25	PMOD0_3_LS	LVCMOS12	U41.5	U41.16	PMOD0_3	J52.7
K23	PMOD0_4_LS	LVCMOS12	U41.6	U41.15	PMOD0_4	J52.2
K21	PMOD0_5_LS	LVCMOS12	U41.7	U41.14	PMOD0_5	J52.4
L24	PMOD0_6_LS	LVCMOS12	U41.8	U41.13	PMOD0_6	J52.6
H25	PMOD0_7_LS	LVCMOS12	U41.9	U41.12	PMOD0_7	J52.8

For more information about PMOD connector compatible PMOD modules, see [Ref 24].

Switches

[Figure 1-2, callouts 27, 30]

The VCU110 evaluation board includes a power on-off slide switch and a configuration pushbutton switch:

- Power on/off slide switch SW1 (callout 30)
- FPGA PROG_B SW4, active-Low (callout 27)

Power On/Off Slide Switch SW1

[Figure 1-2, callout 30]

The VCU110 board power switch is SW1. Sliding the switch actuator from the off to on position applies 12VDC power from the power input connector J15. Green LED DS26 illuminates when the VCU110 board 12V power is on. See the VCU110 Board Power System section for details on the onboard power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J15 on the VCU110 evaluation board. The ATX 6-pin connector has a different pin out than J15. Connecting an ATX 6-pin connector into J15 will damage the VCU110 evaluation board and void the board warranty.*

The VCU110 Evaluation Kit provides the adapter cable shown in Figure 1-23 for powering the VCU110 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to Sourcegate Technologies part number is AZCBL-WH-1109.

Figure 1-23: **ATX Power Supply Adapter Cable**

For more information on ordering this cable, see the Sourcegate Technologies website [Ref 32].

Figure 1-24 shows the power connector J15, power switch SW1 and indicator LED DS26.

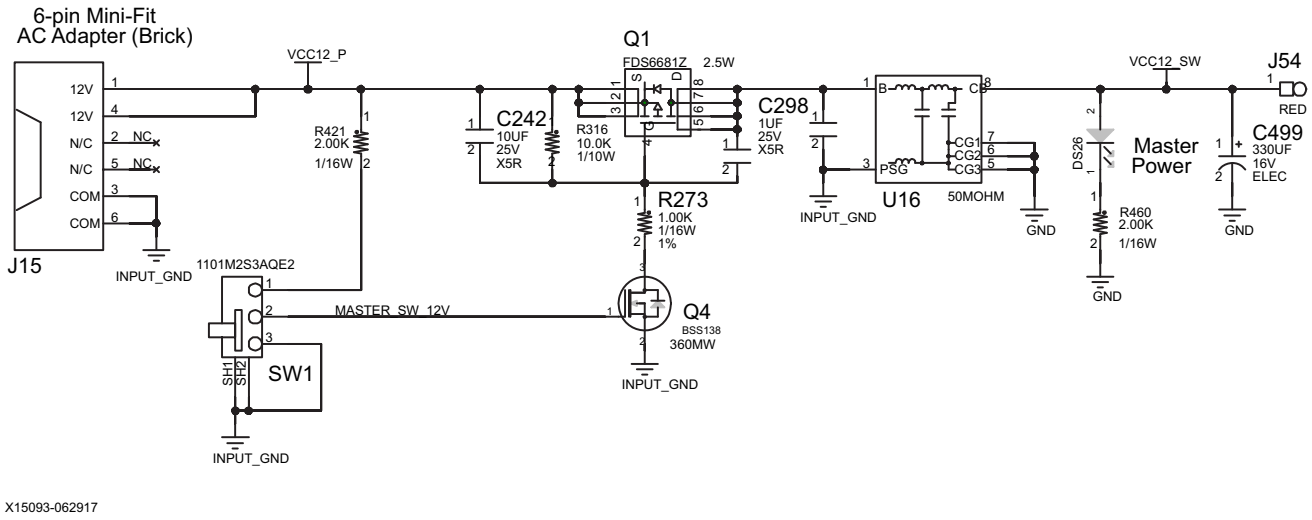

Figure 1-24: **Power On/Off Switch SW1**

Program_B Pushbutton Switch

[Figure 1-2, callout 27]

Switch SW4 grounds the XCVU190 FPGA U1 PROGRAM_B pin when pressed. This action clears the FPGA programmable logic configuration. The FPGA_PROG_B signal is connected to XCVU190 FPGA U1 pin AE14.

For further configuration details, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

Figure 1-25 shows the PROG_B pushbutton SW4.

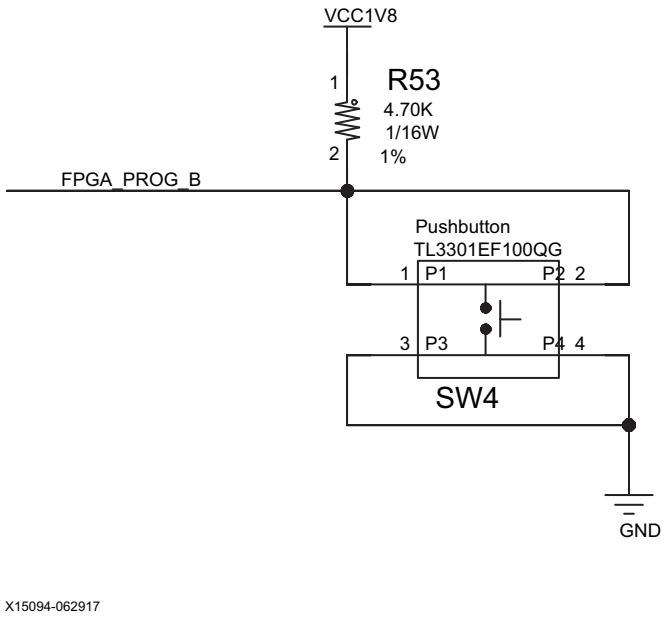

Figure 1-25: **Program_B Pushbutton Switch SW4**

Samtec BULLSEYE1 Connector

[Figure 1-2, callout 40]

The VCU110 board provides two compact, multi-connector surface mount pad patterns. Each pad pattern implements 20 connections configured on the VCU110 board as 10 differential pairs. BULLSEYE1 (J87) is connected to FPGA U1 MGTY bank 126.

Figure 1-26 shows BULLSEYE1 J87.

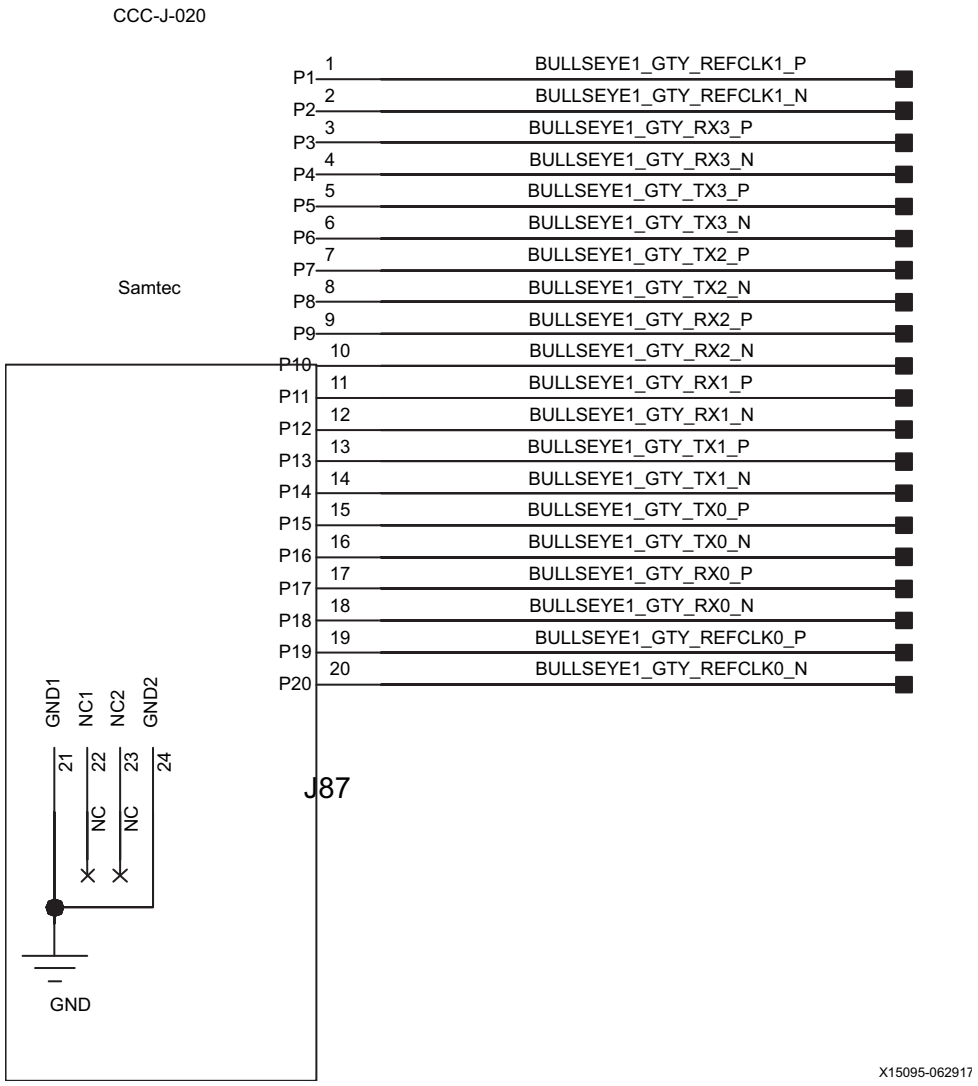

Figure 1-26: **BULLSEYE1 SMA Connector J87**

BULLSEYE1 J87 connections are detailed in Table 1-51.

Table 1-51: **VCU110 BULLSEYE1 SMA J87 to FPGA U1 Connections GTY Quad 126**

BULLSEYE1 J87 Pin Number	Schematic Net Name	FPGA (U1) Pin	FPGA (U1) Pin Name	MGT Quad
15	BULLSEYE1_GTY_TX0_P	AG40	MGTYTXP0_126	GTY Quad 126
16	BULLSEYE1_GTY_TX0_N	AG41	MGTYTXN0_126	
17	BULLSEYE1_GTY_RX0_P	AG45	MGTYRXP0_126	
18	BULLSEYE1_GTY_RX0_N	AG46	MGTYRXN0_126	
13	BULLSEYE1_GTY_TX1_P	AF38	MGTYTXP1_126	
14	BULLSEYE1_GTY_TX1_N	AF39	MGTYTXN1_126	
11	BULLSEYE1_GTY_RX1_P	AF43	MGTYRXP1_126	
12	BULLSEYE1_GTY_RX1_N	AF44	MGTYRXN1_126	
7	BULLSEYE1_GTY_TX2_P	AE40	MGTYTXP2_126	
8	BULLSEYE1_GTY_TX2_N	AE41	MGTYTXN2_126	
9	BULLSEYE1_GTY_RX2_P	AE45	MGTYRXP2_126	
10	BULLSEYE1_GTY_RX2_N	AE46	MGTYRXN2_126	
5	BULLSEYE1_GTY_TX3_P	AD38	MGTYTXP3_126	
6	BULLSEYE1_GTY_TX3_N	AD39	MGTYTXN3_126	
3	BULLSEYE1_GTY_RX3_P	AD43	MGTYRXP3_126	
4	BULLSEYE1_GTY_RX3_N	AD44	MGTYRXN3_126	
19	BULLSEYE1_GTY_REFCLK0_C_P	AC36	MGTREFCLK0P_126	
20	BULLSEYE1_GTY_REFCLK0_C_N	AC37	MGTREFCLK0N_126	
1	BULLSEYE1_GTY_REFCLK1_C_P	AB34	MGTREFCLK1P_126	
2	BULLSEYE1_GTY_REFCLK1_C_N	AB35	MGTREFCLK1N_126	

Samtec BULLSEYE2 Connector

[Figure 1-2, callout 42]

BULLSEYE2 is connected to FPGA U1 MGTY bank 124. Figure 1-27 shows BULLSEYE2 J122.

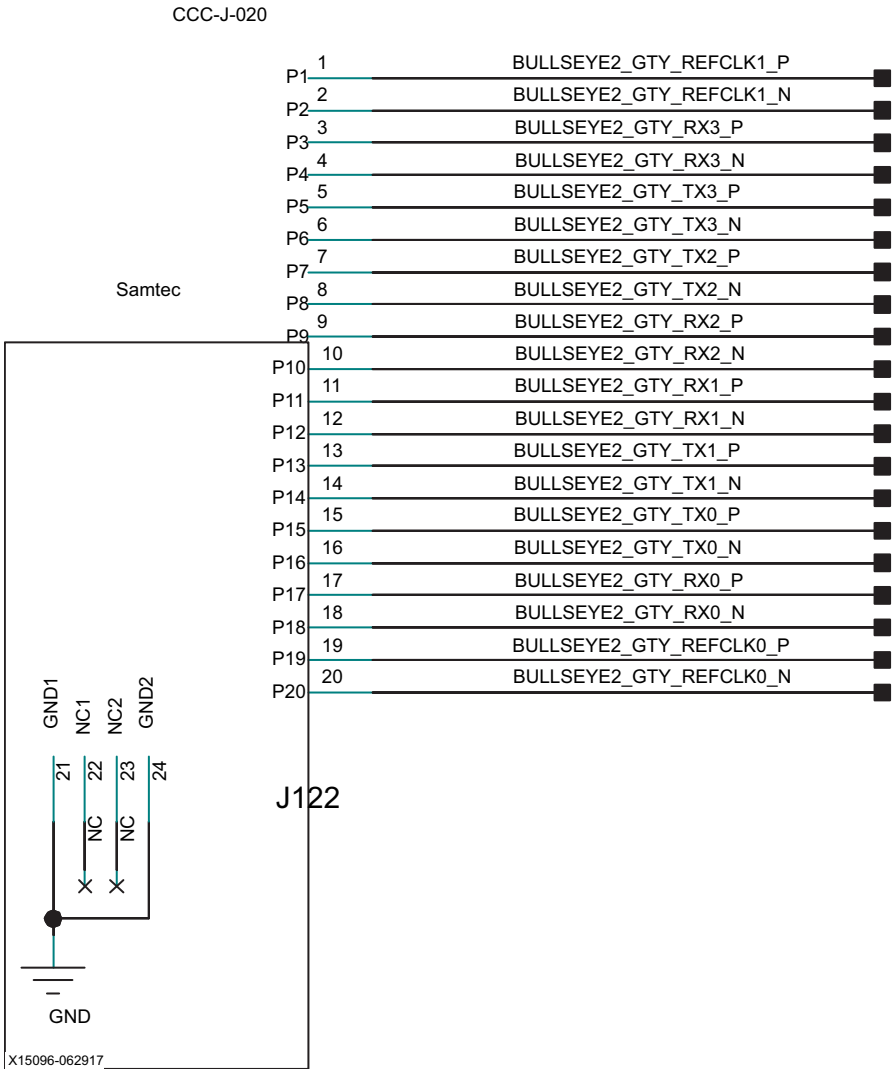

Figure 1-27: **BULLSEYE2 SMA Connector J122**

BULLSEYE2 J122 connections are detailed in Table 1-52.

Table 1-52: **VCU110 BULLSEYE2 SMA J122 to FPGA U1 Connections GTY Quad 124**

BULLSEYE2 J122 Pin Number	Schematic Net Name	FPGA (U1) Pin	FPGA (U1) Pin Name	MGT Quad
15	BULLSEYE2_GTY_TX0_P	AR40	MGTYTXP0_124	GTY Quad 124
16	BULLSEYE2_GTY_TX0_N	AR41	MGTYTXN0_124	
17	BULLSEYE2_GTY_RX0_P	AR45	MGTYRXP0_124	
18	BULLSEYE2_GTY_RX0_N	AR46	MGTYRXN0_124	
13	BULLSEYE2_GTY_TX1_P	AP38	MGTYTXP1_124	
14	BULLSEYE2_GTY_TX1_N	AP39	MGTYTXN1_124	
11	BULLSEYE2_GTY_RX1_P	AP43	MGTYRXP1_124	
12	BULLSEYE2_GTY_RX1_N	AP44	MGTYRXN1_124	
7	BULLSEYE2_GTY_TX2_P	AN40	MGTYTXP2_124	
8	BULLSEYE2_GTY_TX2_N	AN41	MGTYTXN2_124	
9	BULLSEYE2_GTY_RX2_P	AN45	MGTYRXP2_124	
10	BULLSEYE2_GTY_RX2_N	AN46	MGTYRXN2_124	
3	BULLSEYE2_GTY_TX3_P	AM38	MGTYTXP3_124	
4	BULLSEYE2_GTY_TX3_N	AM39	MGTYTXN3_124	
5	BULLSEYE2_GTY_RX3_P	AM43	MGTYRXP3_124	
6	BULLSEYE2_GTY_RX3_N	AM44	MGTYRXN3_124	
19	BULLSEYE2_GTY_REFCLK0_C_P	AG36	MGTREFCLK0P_124	
20	BULLSEYE2_GTY_REFCLK0_C_N	AG37	MGTREFCLK0N_124	
1	BULLSEYE2_GTY_REFCLK1_C_P	AF34	MGTREFCLK1P_124	
2	BULLSEYE2_GTY_REFCLK1_C_N	AF35	MGTREFCLK1N_124	

PCIe Cable Connector

[Figure 1-2, callout 16]

The PCIe cable connector is connected to FPGA U1 GTH Quad 233. Figure 1-28 shows the J136 connector.

IMPORTANT: *The TX_P/N pairs and the CLK_P/N pair are series capacitor coupled to bank 233.*

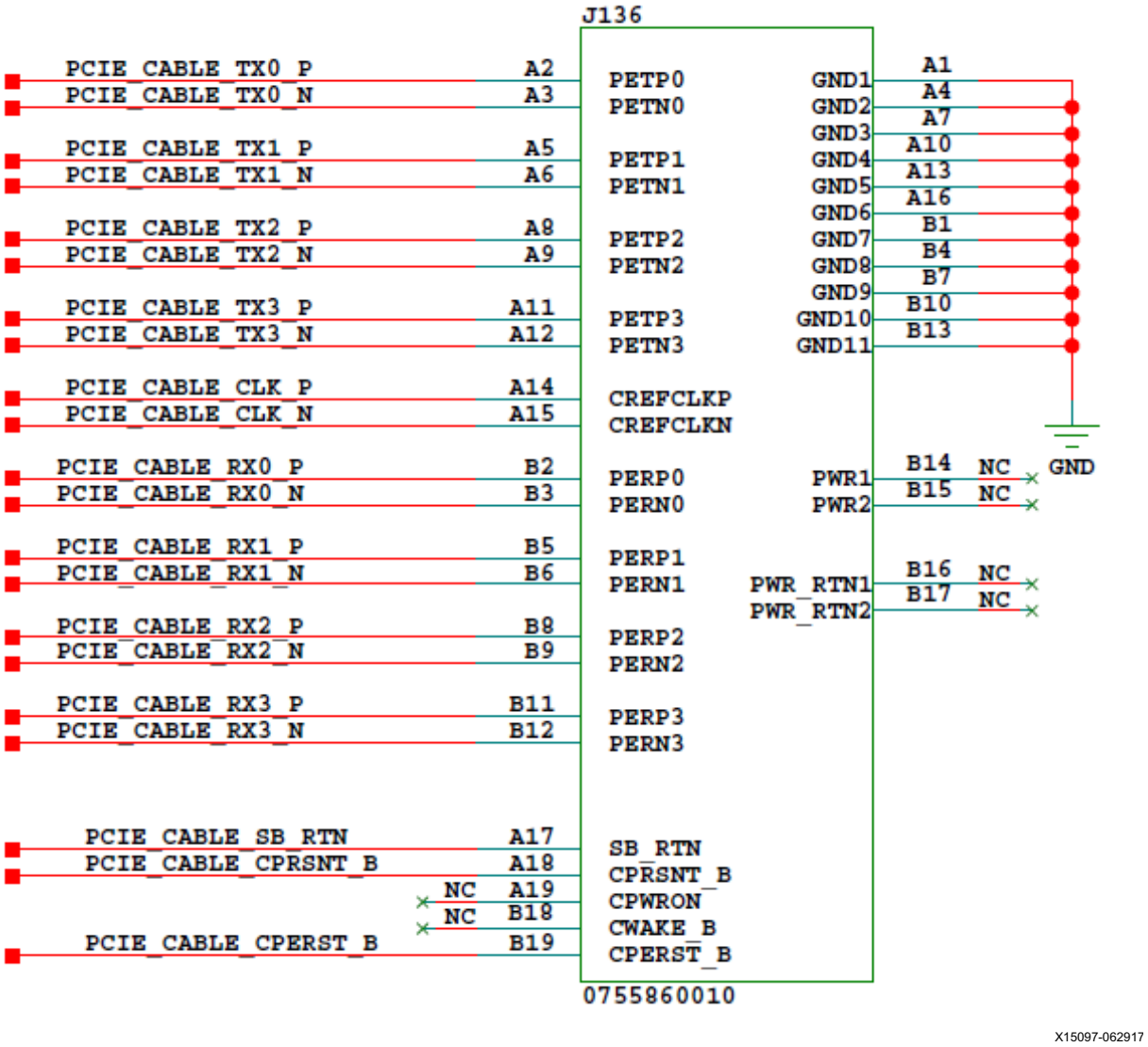

Figure 1-28: **PCIe Cable Connector**

PCIe cable connector J136 connections are detailed in Table 1-53.

For additional information about UltraScale PCIe functionality, see *UltraScale Devices Gen 3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156) [Ref 8]. See [Ref 26] for additional information about the PCI Express standard.

Table 1-53: **VCU110 PCIe Cable Conn. J136 to FPGA U1 Connections GTH Quad 233**

FPGA (U1) Pin Name	FPGA (U1) Pin	Schematic Net Name[1]	Connected Pin Number	Connected Pin Name	Connected Device
MGTHTXP0_233	D9	PCIE_CABLE_TX3_C_P[2]	A11	PETP3	PCIe cable connector J136
MGTHTXN0_233	D8	PCIE_CABLE_TX3_C_N[2]	A12	PETN3	
MGTHRXP0_233	D14	PCIE_CABLE_RX3_P	B11	PERP3	
MGTHRXN0_233	D13	PCIE_CABLE_RX3_N	B12	PERN3	
MGTHTXP1_233	C11	PCIE_CABLE_TX2_C_P[2]	A8	PETP2	
MGTHTXN1_233	C10	PCIE_CABLE_TX2_C_N[2]	A9	PETN2	
MGTHRXP1_233	C16	PCIE_CABLE_RX2_P	B8	PERP2	
MGTHRXN1_233	C15	PCIE_CABLE_RX2_N	B9	PERN2	
MGTHTXP2_233	B9	PCIE_CABLE_TX1_C_P[2]	A5	PETP1	
MGTHTXN2_233	B8	PCIE_CABLE_TX1_C_N[2]	A6	PETN1	
MGTHRXP2_233	B14	PCIE_CABLE_RX1_P	B5	PERP1	
MGTHRXN2_233	B13	PCIE_CABLE_RX1_N	B6	PERN1	
MGTHTXP3_233	A11	PCIE_CABLE_TX0_C_P[2]	A2	PETP0	
MGTHTXN3_233	A10	PCIE_CABLE_TX0_C_N[2]	A3	PETN0	
MGTHRXP3_233	A16	PCIE_CABLE_RX0_P	B2	PERP0	
MGTHRXN3_233	A15	PCIE_CABLE_RX0_N	B3	PERN0	
MGTREFCLK0P_233	J11	PCIE_CABLE_CLK_C_P[2]	A14	CREFCLKP	
MGTREFCLK0N_233	J10	PCIE_CABLE_CLK_C_N[2]	A15	CREFCLKN	

Notes:
1. MGT connections I/O standard not applicable.
2. Series capacitor coupled.

Interlaken Connector

[Figure 1-2, callout 42]

The VCU110 board provides an FCI Interlaken connector at J121. Five FPGA U1 GTY Quads (129-133) implement twenty transmit/receive differential pair channels. The Interlaken connector DATA, CLK and SYNC control signals are connected to FPGA U1 bank 65.

The Interlaken J121 to FPGA U1 connections are detailed in Table 1-54.

Table 1-54: **VCU110 Interlaken Connector J121 Connections**

Interlaken J121 Pin Name	Interlaken J121 Pin Number	Schematic Net Name[2]	FPGA (U1) Pin	FPGA (U1) Pin Name	FPGA U1 Bank
TX0_P	A2	ILKN_TX0_P	R40	MGTYTXP0_129	GTY Quad 129
TX0_N	A3	ILKN_TX0_N	R41	MGTYTXN0_129	
RX0_P	B2	ILKN_RX0_C_P[1]	R45	MGTYRXP0_129	
RX0_N	B3	ILKN_RX0_C_N[1]	R46	MGTYRXN0_129	
TX1_P	C2	ILKN_TX1_P	P38	MGTYTXP1_129	
TX1_N	C3	ILKN_TX1_N	P39	MGTYTXN1_129	
RX1_P	D2	ILKN_RX1_C_P[1]	P43	MGTYRXP1_129	
RX1_N	D3	ILKN_RX1_C_N[1]	P44	MGTYRXN1_129	
TX2_P	A5	ILKN_TX2_P	N40	MGTYTXP2_129	
TX2_N	A6	ILKN_TX2_N	N41	MGTYTXN2_129	
RX2_P	B5	ILKN_RX2_C_P[1]	N45	MGTYRXP2_129	
RX2_N	B6	ILKN_RX2_C_N[1]	N46	MGTYRXN2_129	
TX3_P	C5	ILKN_TX3_P	M38	MGTYTXP3_129	
TX3_N	C6	ILKN_TX3_N	M39	MGTYTXN3_129	
RX3_P	D5	ILKN_RX3_C_P[1]	M43	MGTYRXP3_129	
RX3_N	D6	ILKN_RX3_C_N[1]	M44	MGTYRXN3_129	
TX4_P	A8	ILKN_TX4_P	L40	MGTYTXP0_130	GTY Quad 130
TX4_N	A9	ILKN_TX4_N	L41	MGTYTXN0_130	
RX4_P	B8	ILKN_RX4_C_P[1]	L45	MGTYRXP0_130	
RX4_N	B9	ILKN_RX4_C_N[1]	L46	MGTYRXN0_130	
TX5_P	C8	ILKN_TX5_P	K38	MGTYTXP1_130	
TX5_N	C9	ILKN_TX5_N	K39	MGTYTXN1_130	
RX5_P	D8	ILKN_RX5_C_P[1]	K43	MGTYRXP1_130	
RX5_N	D9	ILKN_RX5_C_N[1]	K44	MGTYRXN1_130	
TX6_P	F2	ILKN_TX6_P	J40	MGTYTXP2_130	
TX6_N	F3	ILKN_TX6_N	J41	MGTYTXN2_130	
RX6_P	G2	ILKN_RX6_C_P[1]	J45	MGTYRXP2_130	
RX6_N	G3	ILKN_RX6_C_N[1]	J46	MGTYRXN2_130	
TX7_P	H2	ILKN_TX7_P	H38	MGTYTXP3_130	
TX7_N	H3	ILKN_TX7_N	H39	MGTYTXN3_130	
RX7_P	J2	ILKN_RX7_C_P[1]	H43	MGTYRXP3_130	
RX7_N	J3	ILKN_RX7_C_N[1]	H44	MGTYRXN3_130	

Table 1-54: **VCU110 Interlaken Connector J121 Connections *(Cont'd)***

Interlaken J121 Pin Name	Interlaken J121 Pin Number	Schematic Net Name[2]	FPGA (U1) Pin	FPGA (U1) Pin Name	FPGA U1 Bank
TX8_P	F5	ILKN_TX8_P	G40	MGTYTXP0_131	GTY Quad 131
TX8_N	F6	ILKN_TX8_N	G41	MGTYTXN0_131	
RX8_P	G5	ILKN_RX8_C_P[1]	G45	MGTYRXP0_131	
RX8_N	G6	ILKN_RX8_C_N[1]	G46	MGTYRXN0_131	
TX9_P	H5	ILKN_TX9_P	F38	MGTYTXP1_131	
TX9_N	H6	ILKN_TX9_N	F39	MGTYTXN1_131	
RX9_P	J5	ILKN_RX9_C_P[1]	F43	MGTYRXP1_131	
RX9_N	J6	ILKN_RX9_C_N[1]	F44	MGTYRXN1_131	
TX10_P	F8	ILKN_TX10_P	G36	MGTYTXP2_131	
TX10_N	F9	ILKN_TX10_N	G37	MGTYTXN2_131	
RX10_P	G8	ILKN_RX10_C_P[1]	G31	MGTYRXP2_131	
RX10_N	G9	ILKN_RX10_C_N[1]	G32	MGTYRXN2_131	
TX11_P	H8	ILKN_TX11_P	F34	MGTYTXP3_131	
TX11_N	H9	ILKN_TX11_N	F35	MGTYTXN3_131	
RX11_P	J8	ILKN_RX11_C_P[1]	E31	MGTYRXP3_131	
RX11_N	J9	ILKN_RX11_C_N[1]	E32	MGTYRXN3_131	
TX12_P	F11	ILKN_TX12_P	E40	MGTYTXP0_132	GTY Quad 132
TX12_N	F12	ILKN_TX12_N	E41	MGTYTXN0_132	
RX12_P	G11	ILKN_RX12_C_P[1]	E45	MGTYRXP0_132	
RX12_N	G12	ILKN_RX12_C_N[1]	E46	MGTYRXN0_132	
TX13_P	H11	ILKN_TX13_P	E36	MGTYTXP1_132	
TX13_N	H12	ILKN_TX13_N	E37	MGTYTXN1_132	
RX13_P	J11	ILKN_RX13_C_P[1]	D43	MGTYRXP1_132	
RX13_N	J12	ILKN_RX13_C_N[1]	D44	MGTYRXN1_132	
TX14_P	F14	ILKN_TX14_P	C40	MGTYTXP2_132	
TX14_N	F15	ILKN_TX14_N	C41	MGTYTXN2_132	
RX14_P	J14	ILKN_RX14_C_P[1]	C45	MGTYRXP2_132	
RX14_N	J15	ILKN_RX14_C_N[1]	C46	MGTYRXN2_132	
TX15_P	H14	ILKN_TX15_P	A40	MGTYTXP3_132	
TX15_N	H15	ILKN_TX15_N	A41	MGTYTXN3_132	
RX15_P	J14	ILKN_RX15_C_P[1]	B43	MGTYRXP3_132	
RX15_N	J15	ILKN_RX15_C_N[1]	B44	MGTYRXN3_132	

Table 1-54: **VCU110 Interlaken Connector J121 Connections *(Cont'd)***

Interlaken J121 Pin Name	Interlaken J121 Pin Number	Schematic Net Name[2]	FPGA (U1) Pin	FPGA (U1) Pin Name	FPGA U1 Bank
TX16_P	A11	ILKN_TX16_P	D38	MGTYTXP0_133	GTY Quad 133
TX16_N	A12	ILKN_TX16_N	D39	MGTYTXN0_133	
RX16_P	J14	ILKN_RX16_C_P[1]	D33	MGTYRXP0_133	
RX16_N	J15	ILKN_RX16_C_N[1]	D34	MGTYRXN0_133	
TX17_P	C11	ILKN_TX17_P	C36	MGTYTXP1_133	
TX17_N	C12	ILKN_TX17_N	C37	MGTYTXN1_133	
RX17_P	D11	ILKN_RX17_C_P[1]	C31	MGTYRXP1_133	
RX17_N	D12	ILKN_RX17_C_N[1]	C32	MGTYRXN1_133	
TX18_P	A14	ILKN_TX18_P	B38	MGTYTXP2_133	
TX18_N	A15	ILKN_TX18_N	B39	MGTYTXN2_133	
RX18_P	B14	ILKN_RX18_C_P[1]	B33	MGTYRXP2_133	
RX18_N	B15	ILKN_RX18_C_N[1]	B34	MGTYRXN2_133	
TX19_P	C14	ILKN_TX19_P	A36	MGTYTXP3_133	
TX19_N	C15	ILKN_TX19_N	A37	MGTYTXN3_133	
RX19_P	D14	ILKN_RX19_C_P[1]	A31	MGTYRXP3_133	
RX19_N	D15	ILKN_RX19_C_N[1]	A32	MGTYRXN3_133	
TX20_P	A17	NA		NA	NA
TX20_N	A18	NA		NA	
RX20_P	B17	NA		NA	
RX20_N	B18	NA		NA	
TX21_P	C17	NA		NA	
TX21_N	C18	NA		NA	
RX21_P	D17	NA		NA	
RX21_N	D18	NA		NA	
FC_TX_SYNC	J17	ILKN_FC_TX_SYNC[3]	AM19	IO_L3P_T0L_N4	65
FC_RX_SYNC	J18	ILKN_FC_RX_SYNC[3]	AN20	IO_L2P_T0L_N2	
FC_TX_DATA	H17	ILKN_FC_TX_DATA[3]	AN21	IO_L4N_T0U_N7	
FC_RX_DATA	H18	ILKN_FC_RX_DATA[3]	AN19	IO_L3N_T0L_N5	
FC_TX_CLK	G17	ILKN_FC_TX_CLK[3]	AW17	IO_L11N_T1U_N9	
FC_RX_CLK	F17	ILKN_FC_RX_CLK[3]	AW18	IO_L11P_T1U_N8	

Table 1-54: **VCU110 Interlaken Connector J121 Connections *(Cont'd)***

Interlaken J121 Pin Name	Interlaken J121 Pin Number	Schematic Net Name[2]	FPGA (U1) Pin	FPGA (U1) Pin Name	FPGA U1 Bank
SPARE1	G18	GND	NA	NA	NA
SPARE2	F18	GND	NA	NA	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.
3. Level-shifted via U185 and U186.

The Interlaken protocol definition and recommended connector pinouts are in documents located on the Interlaken Alliance website [Ref 33].

For the Interlaken Protocol, refer to the Interlaken Look-Aside Protocol Definition v1.x, and for connector pin-outs, refer to Interlaken Interop Recommendations v1.x. The protocol definition document also discusses the flow control functions provided by the TX and RX FC_CLK, FC_DATA and FC_SYNC connector pins.

ExaMAX Backplane Connector

[Figure 1-2, callout 43]

The VCU110 board provides an FCI ExaMAX backplane connector at J116. Two FPGA U1 GTY Quads (121 and 120) implement eight differential transmit/receive pair channels.

The ExaMAX J116 to FPGA U1 connections are detailed in Table 1-55.

Table 1-55: **VCU110 ExaMAX J116 to FPGA U1 GTY Quads 121-120 Connections**

ExaMAX J116 Pin Name	ExaMAX J116 Pin Number	Schematic Net Name[1]	FPGA (U1) Pin	FPGA (U1) Pin Name	MGT Quad
TX1_P	K4	EXAMAX_TX1_P	AY38	MGTYTXP3_121	GTY Quad 121
TX1_N	L4	EXAMAX_TX1_N	AY39	MGTYTXN3_121	
RX1_P	B4	EXAMAX_RX1_P	AY43	MGTYRXP3_121	
RX1_N	C4	EXAMAX_RX1_N	AY44	MGTYRXN3_121	
TX2_P	H4	EXAMAX_TX2_P	BA40	MGTYTXP2_121	
TX2_N	I4	EXAMAX_TX2_N	BA41	MGTYTXN2_121	
RX2_P	E4	EXAMAX_RX2_P	BA45	MGTYRXP2_121	
RX2_N	F4	EXAMAX_RX2_N	BA46	MGTYRXN2_121	
TX3_P	L5	EXAMAX_TX3_P	BB38	MGTYTXP1_121	
TX3_N	M5	EXAMAX_TX3_N	BB39	MGTYTXN1_121	
RX3_P	C5	EXAMAX_RX3_P	BB43	MGTYRXP1_121	
RX3_N	D5	EXAMAX_RX3_N	BB44	MGTYRXN1_121	
TX4_P	I5	EXAMAX_TX4_P	BC40	MGTYTXP0_121	
TX4_N	J5	EXAMAX_TX4_N	BC41	MGTYTXN0_121	
RX4_P	F5	EXAMAX_RX4_P	BC45	MGTYRXP0_121	
RX4_N	G5	EXAMAX_RX4_N	BC46	MGTYRXN0_121	

Table 1-55: **VCU110 ExaMAX J116 to FPGA U1 GTY Quads 121-120 Connections *(Cont'd)***

ExaMAX J116 Pin Name	ExaMAX J116 Pin Number	Schematic Net Name[1]	FPGA (U1) Pin	FPGA (U1) Pin Name	MGT Quad
TX5_P	K6	EXAMAX_TX5_P	AT38	MGTYTXP3_120	GTY Quad 120
TX5_N	L6	EXAMAX_TX5_N	AT39	MGTYTXN3_120	
RX5_P	B6	EXAMAX_RX5_P	AT43	MGTYRXP3_120	
RX5_N	C6	EXAMAX_RX5_N	AT44	MGTYRXN3_120	
TX6_P	H6	EXAMAX_TX6_P	AU40	MGTYTXP2_120	
TX6_N	I6	EXAMAX_TX6_N	AU41	MGTYTXN2_120	
RX6_P	E6	EXAMAX_RX6_P	AU45	MGTYRXP2_120	
RX6_N	F6	EXAMAX_RX6_N	AU46	MGTYRXN2_120	
TX7_P	L7	EXAMAX_TX7_P	AV38	MGTYTXP1_120	
TX7_N	M7	EXAMAX_TX7_N	AV39	MGTYTXN1_120	
RX7_P	C7	EXAMAX_RX7_P	AV43	MGTYRXP1_120	
RX7_N	D7	EXAMAX_RX7_N	AV44	MGTYRXN1_120	
TX8_P	I7	EXAMAX_TX8_P	AW40	MGTYTXP0_120	
TX8_N	J7	EXAMAX_TX8_N	AW41	MGTYTXN0_120	
RX8_P	F7	EXAMAX_RX8_P	AW45	MGTYRXP0_120	
RX8_N	G7	EXAMAX_RX8_N	AW46	MGTYRXN0_120	

Notes:
1. MGT connections I/O standard not applicable.

FPGA Mezzanine Card (FMC) Interface

[Figure 1-2, callouts 33, 34]

The VCU110 evaluation board supports the VITA 57.1 FPGA Mezzanine Card (FMC) specification by providing subset implementations of high pin count connectors at J22 (HPC0) and J2 (HPC1). HPC connectors use a 10 x 40 form factor, populated with 400 pins. The connectors are keyed so that a mezzanine card, when installed in either of these FMC connectors on the VCU110 evaluation board, faces away from the board.

The Samtec connector system is rated for signaling speeds up to 9 GHz (18 Gb/s) based on a –3 dB insertion loss point within a two-level signaling environment.

Connector Type

- Samtec SEAF Series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector.

  More information about SEAF series connectors is available at the Samtec website [Ref 34].

More information about the VITA 57.1 FMC specification is available at the VITA Marketing Alliance site [Ref 35].

- The 400-pin HPC connector defined by the FMC specification (Figure B-1) provides connectivity for up to:
  - 160 single-ended or 80 differential user-defined signals
  - 10 GT transceivers
  - 2 GT clocks
  - 4 differential clocks
  - 159 ground and 15 power connections

FMC HPC0 Connector J22

[Figure 1-2, callout 33]

The HPC connector at J22 implements a subset of the full FMC HPC connectivity:

- 11 differential user-defined pairs (11 LA pairs: LA[00:10])
- 8 GT transceivers
- 2 GT clocks
- 1 differential clock
- 159 ground and 15 power connections

The VCU110 board FMC V_{ADJ} voltage VADJ_1V8_FPGA for the J22 and J2 FMC connectors is determined by the MAX15301 U30 voltage regulator described in the VCU110 Board Power System section.

The HPC0 J22 connections to FPGA U1 are shown in Table 1-56 through Table 1-60.

Table 1-56: **J22 VITA 57.1 FMC HPC0 Sections A and B to FPGA U1 Connections**

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
A2	FMC_HPC0_DP1_M2C_P	(1)	BD14	B1	NA		
A3	FMC_HPC0_DP1_M2C_N	(1)	BD13	B4	NA		
A6	FMC_HPC0_DP2_M2C_P	(1)	BF4	B5	NA		
A7	FMC_HPC0_DP2_M2C_N	(1)	BF3	B8	NA		
A10	FMC_HPC0_DP3_M2C_P	(1)	BD4	B9	NA		
A11	FMC_HPC0_DP3_M2C_N	(1)	BD3	B12	FMC_HPC0_DP7_M2C_P	(1)	AY4
A14	FMC_HPC0_DP4_M2C_P	(1)	BC2	B13	FMC_HPC0_DP7_M2C_N	(1)	AY3

Table 1-56: **J22 VITA 57.1 FMC HPC0 Sections A and B to FPGA U1 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
A15	FMC_HPC0_DP4_M2C_N	(1)	BC1	B16	FMC_HPC0_DP6_M2C_P	(1)	BA2
A18	FMC_HPC0_DP5_M2C_P	(1)	BB4	B17	FMC_HPC0_DP6_M2C_N	(1)	BA1
A19	FMC_HPC0_DP5_M2C_N	(1)	BB3	B20	FMC_HPC0_GBTCLK1_M2C_P(2)	(1)	AK13
A22	FMC_HPC0_DP1_C2M_P	(1)	BE11	B21	FMC_HPC0_GBTCLK1_M2C_N(2)	(1)	AK12
A23	FMC_HPC0_DP1_C2M_N	(1)	BE10	B24	NA		
A26	FMC_HPC0_DP2_C2M_P	(1)	BE7	B25	NA		
A27	FMC_HPC0_DP2_C2M_N	(1)	BE6	B28	NA		
A30	FMC_HPC0_DP3_C2M_P	(1)	BD9	B29	NA		
A31	FMC_HPC0_DP3_C2M_N	(1)	BD8	B32	FMC_HPC0_DP7_C2M_P	(1)	AY9
A34	FMC_HPC0_DP4_C2M_P	(1)	BC7	B33	FMC_HPC0_DP7_C2M_N	(1)	AY8
A35	FMC_HPC0_DP4_C2M_N	(1)	BC6	B36	FMC_HPC0_DP6_C2M_P	(1)	BA7
A38	FMC_HPC0_DP5_C2M_P	(1)	BB9	B37	FMC_HPC0_DP6_C2M_N	(1)	BA6
A39	FMC_HPC0_DP5_C2M_N	(1)	BB8	B40	NA	NA	

Notes:

1. No I/O standards are associated with MGT connections.
2. Series capacitor coupled.

Table 1-57: **J22 VITA 57.1 FMC HPC0 Sections C and D to FPGA U1 Connections**

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC 0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C2	FMC_HPC0_DP0_C2M_P	(1)	BF9	D1	VADJ_1V8_PGOOD(3)	LVCMOS18	AP18
C3	FMC_HPC0_DP0_C2M_N	(1)	BF8	D4	FMC_HPC0_GBTCLK0_M2C_P(2)	(1)	AL11
C6	FMC_HPC0_DP0_M2C_P	(1)	BF14	D5	FMC_HPC0_GBTCLK0_M2C_N(2)	(1)	AL10
C7	FMC_HPC0_DP0_M2C_N	(1)	BF13	D8	FMC_HPC0_LA01_CC_P	LVDS	AY32
C10	FMC_HPC0_LA06_P	LVDS	BD30	D9	FMC_HPC0_LA01_CC_N	LVDS	BA32
C11	FMC_HPC0_LA06_N	LVDS	BE30	D11	FMC_HPC0_LA05_P	LVDS	BC29
C14	FMC_HPC0_LA10_P	LVDS	AR32	D12	FMC_HPC0_LA05_N	LVDS	BC30
C15	FMC_HPC0_LA10_N	LVDS	AT32	D14	FMC_HPC0_LA09_P	LVDS	BC31
C18	NA	NA		D15	FMC_HPC0_LA09_N	LVDS	BD31
C19	NA	NA		D17	NA	NA	
C22	NA	NA		D18	NA	NA	
C23	NA	NA		D20	NA	NA	
C26	NA	NA		D21	NA	NA	

Table 1-57: **J22 VITA 57.1 FMC HPC0 Sections C and D to FPGA U1 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC 0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C27	NA	NA		D23	NA	NA	
C30	FMC_HPC0_IIC_SCL	U80.9		D24	NA	NA	
C31	FMC_HPC0_IIC_SDA	U80.8		D26	NA	NA	
C34	GA0 = 0 = GND			D27	NA	NA	
C35	VCC12_SW			D29	FMC_HPC0_TCK_BUF		U19.17
C37	VCC12_SW			D30	FPGA_TDO_FMC_TDI_BUF		U19.21
C39	UTIL_3V3			D31	FMC_HPC0_TDO_HPC1_TDI		U132.1
				D32	VCC3V3		
				D33	FMC_HPC0_TMS_BUF		U19.20
				D34	NA		
				D35	GA1 = 0 = GND		
				D36	UTIL_3V3		
				D38	UTIL_3V3		
				D40	UTIL_3V3		

Notes:

1. No I/O standards are associated with MGT connections.
2. Series capacitor coupled.
3. VADJ_1V8_PGOOD level-shifted from 3.3V to 1.8V at TXS0108E U44.

Table 1-58: **J22 VITA 57.1 FMC HPC0 Sections E and F to FPGA U1 Connections**

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
E2	NA	NA		F1	FMC_HPC0_PG_M2C(1)	LVCMOS18	BD20
E3	NA	NA		F4	NA	NA	
E6	NA	NA		F5	NA	NA	
E7	NA	NA		F7	NA	NA	
E9	NA	NA		F8	NA	NA	
E10	NA	NA		F10	NA	NA	
E12	NA	NA		F11	NA	NA	
E13	NA	NA		F13	NA	NA	
E15	NA	NA		F14	NA	NA	
E16	NA	NA		F16	NA	NA	
E18	NA	NA		F17	NA	NA	

Table 1-58: **J22 VITA 57.1 FMC HPC0 Sections E and F to FPGA U1 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
E19	NA	NA		F19	NA	NA	
E21	NA	NA		F20	NA	NA	
E22	NA	NA		F22	NA	NA	
E24	NA	NA		F23	NA	NA	
E25	NA	NA		F25	NA	NA	
E27	NA	NA		F26	NA	NA	
E28	NA	NA		F28	NA	NA	
E30	NA	NA		F29	NA	NA	
E31	NA	NA		F31	NA	NA	
E33	NA	NA		F32	NA	NA	
E34	NA	NA		F34	NA	NA	
E36	NA	NA		F35	NA	NA	
E37	NA	NA		F37	NA	NA	
E39	VADJ _1V8_FPGA			F38	NA	NA	
				F40	VADJ _1V8_FPGA		

Notes:

1. FMC_HPC0_PG_M2C level-shifted from 3.3V to 1.8V at TXS0108E U44.

Table 1-59: **J22 VITA 57.1 FMC HPC0 Sections G and H to FPGA U1 Connections**

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G2	NA	NA		H1	FMC_HPC0_VREF_A_M2C(3)	NA	
G3	NA	NA		H2	FMC_HPC0_PRSNT_M2C_B(1)(2)	LVCMOS18	R13
G6	FMC_HPC0_LA00_CC_P	LVDS	AY34	H4	FMC_HPC0_CLK0_M2C_P	LVDS	AW33
G7	FMC_HPC0_LA00_CC_N	LVDS	AY35	H5	FMC_HPC0_CLK0_M2C_N	LVDS	AY33
G9	FMC_HPC0_LA03_P	LVDS	BA34	H7	FMC_HPC0_LA02_P	LVDS	BA36
G10	FMC_HPC0_LA03_N	LVDS	BB34	H8	FMC_HPC0_LA02_N	LVDS	BB36
G12	FMC_HPC0_LA08_P	LVDS	BE29	H10	FMC_HPC0_LA04_P	LVDS	BB32
G13	FMC_HPC0_LA08_N	LVDS	BF29	H11	FMC_HPC0_LA04_N	LVDS	BB33
G15	NA	NA		H13	FMC_HPC0_LA07_P	LVDS	BA31
G16	NA	NA		H14	FMC_HPC0_LA07_N	LVDS	BB31
G18	NA	NA		H16	NA	NA	

Table 1-59: **J22 VITA 57.1 FMC HPC0 Sections G and H to FPGA U1 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G19	NA	NA		H17	NA	NA	
G21	NA	NA		H19	NA	NA	
G22	NA	NA		H20	NA	NA	
G24	NA	NA		H22	NA	NA	
G25	NA	NA		H23	NA	NA	
G27	NA	NA		H25	NA	NA	
G28	NA	NA		H26	NA	NA	
G30	NA	NA		H28	NA	NA	
G31	NA	NA		H29	NA	NA	
G33	NA	NA		H31	NA	NA	
G34	NA	NA		H32	NA	NA	
G36	NA	NA		H34	NA	NA	
G37	NA	NA		H35	NA	NA	
G39	VADJ _1V8_FPGA			H37	NA	NA	
				H38	NA	NA	
				H40	VADJ _1V8_FPGA		

Notes:

1. FMC_HPC0_PRSNT_M2C_B level-shifted from 3.3V to 1.8V at U44.
2. FMC_HPC0_PRSNT_M2C_B level-shifted from 3.3V to 1.8V at TXS0108E U109, connected to U111 pin R13.
3. FMC_HPC0_VREF_A_M2C is the source of U1 bank 68 Vref pin AM32 connected via DNP series resistor R1674, and U1 bank 84 Vref pin AM17 via DNP resistor R796.

Table 1-60: **J22 VITA 57.1 FMC HPC0 Sections J and K to FPGA U1 Connections**

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
J2	NA	NA		K1	NA	NA	
J3	NA	NA		K4	NA	NA	
J6	NA	NA		K5	NA	NA	
J7	NA	NA		K7	NA	NA	
J9	NA	NA		K8	NA	NA	
J10	NA	NA		K10	NA	NA	
J12	NA	NA		K11	NA	NA	
J13	NA	NA		K13	NA	NA	

Table 1-60: **J22 VITA 57.1 FMC HPC0 Sections J and K to FPGA U1 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin		J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
J15	NA	NA			K14	NA	NA	
J16	NA	NA			K16	NA	NA	
J18	NA	NA			K17	NA	NA	
J19	NA	NA			K19	NA	NA	
J21	NA	NA			K20	NA	NA	
J22	NA	NA			K22	NA	NA	
J24	NA	NA			K23	NA	NA	
J25	NA	NA			K25	NA	NA	
J27	NA	NA			K26	NA	NA	
J28	NA	NA			K28	NA	NA	
J30	NA	NA			K29	NA	NA	
J31	NA	NA			K31	NA	NA	
J33	NA	NA			K32	NA	NA	
J34	NA	NA			K34	NA	NA	
J36	NA	NA			K35	NA	NA	
J37	NA	NA			K37	NA	NA	
J39	NA	NA			K38	NA	NA	
J39	NA	NA			K40	NA	NA	

FMC HPC1 Connector J2

[Figure 1-2, callout 34]

The HPC connector at J2 implements a subset of the full FMC HPC connectivity:

- 11 differential user-defined pairs (11 LA pairs: LA[00:10])
- 8 GT transceivers
- 2 GT clocks
- 1 differential clock
- 159 ground and 15 power connections

The HPC1 J2 connections to FPGA U1 are shown in Table 1-61 through Table 1-65.

Table 1-61: **J2 VITA 57.1 FMC HPC1 Sections A and B to FPGA U1 Connections**

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
A2	FMC_HPC1_DP1_M2C_P	(1)	AP4	B1	NA	NA	
A3	FMC_HPC1_DP1_M2C_N	(1)	AP3	B4	NA	NA	
A6	FMC_HPC1_DP2_M2C_P	(1)	AN2	B5	NA	NA	
A7	FMC_HPC1_DP2_M2C_N	(1)	AN1	B8	NA	NA	
A10	FMC_HPC1_DP3_M2C_P	(1)	AM4	B9	NA	NA	
A11	FMC_HPC1_DP3_M2C_N	(1)	AM3	B12	FMC_HPC1_DP7_M2C_P	(1)	AT4
A14	FMC_HPC1_DP4_M2C_P	(1)	AW2	B13	FMC_HPC1_DP7_M2C_N	(1)	AT3
A15	FMC_HPC1_DP4_M2C_N	(1)	AW1	B16	FMC_HPC1_DP6_M2C_P	(1)	AU2
A18	FMC_HPC1_DP5_M2C_P	(1)	AV4	B17	FMC_HPC1_DP6_M2C_N	(1)	AU1
A19	FMC_HPC1_DP5_M2C_N	(1)	AV3	B20	FMC_HPC1_GBTCLK1_M2C_P	(1)	AF13
A22	FMC_HPC1_DP1_C2M_P	(1)	AP9	B21	FMC_HPC1_GBTCLK1_M2C_N	(1)	AF12
A23	FMC_HPC1_DP1_C2M_N	(1)	AP8	B24	NA	NA	
A26	FMC_HPC1_DP2_C2M_P	(1)	AN7	B25	NA	NA	
A27	FMC_HPC1_DP2_C2M_N	(1)	AN6	B28	NA	NA	
A30	FMC_HPC1_DP3_C2M_P	(1)	AM9	B29	NA	NA	
A31	FMC_HPC1_DP3_C2M_N	(1)	AM8	B32	FMC_HPC1_DP7_C2M_P	(1)	AT9
A34	FMC_HPC1_DP4_C2M_P	(1)	AW7	B33	FMC_HPC1_DP7_C2M_N	(1)	AT8
A35	FMC_HPC1_DP4_C2M_N	(1)	AW6	B36	FMC_HPC1_DP6_C2M_P	(1)	AU2
A38	FMC_HPC1_DP5_C2M_P	(1)	AV9	B37	FMC_HPC1_DP6_C2M_N	(1)	AU1
A39	FMC_HPC1_DP5_C2M_N	(1)	AV8	B40	NA	NA	

Notes:
1. No I/O standards are associated with MGT connections.

Table 1-62: **J2 VITA 57.1 FMC HPC1 Sections C and D to FPGA U1 Connections**

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C2	FMC_HPC1_DP0_C2M_P	(1)	AR7	D1	VADJ_1V8_PGOOD	LVCMOS18	AP18
C3	FMC_HPC1_DP0_C2M_N	(1)	AR6	D4	FMC_HPC1_GBTCLK0_M2C_P	(1)	AG11
C6	FMC_HPC1_DP0_M2C_P	(1)	AR2	D5	FMC_HPC1_GBTCLK0_M2C_N	(1)	AG10
C7	FMC_HPC1_DP0_M2C_N	(1)	AR1	D8	FMC_HPC1_LA01_CC_P	LVCMOS18	AR35
C10	FMC_HPC1_LA06_P	LVCMOS18	AR36	D9	FMC_HPC1_LA01_CC_N	LVCMOS18	AT35

Table 1-62: **J2 VITA 57.1 FMC HPC1 Sections C and D to FPGA U1 Connections *(Cont'd)***

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C11	FMC_HPC1_LA06_N	LVCMOS18	AT36	D11	FMC_HPC1_LA05_P	LVCMOS18	BC29
C14	FMC_HPC1_LA10_P	LVCMOS18	AR32	D12	FMC_HPC1_LA05_N	LVCMOS18	AU32
C15	FMC_HPC1_LA10_N	LVCMOS18	AT32	D14	FMC_HPC1_LA09_P	LVCMOS18	AV31
C18	NA	NA		D15	FMC_HPC1_LA09_N	LVCMOS18	AW31
C19	NA	NA		D17	NA	NA	
C22	NA	NA		D18	NA	NA	
C23	NA	NA		D20	NA	NA	
C26	NA	NA		D21	NA	NA	
C27	NA	NA		D23	NA	NA	
C30	FMC_HPC1_IIC_SCL		U80.13	D24	NA	NA	
C31	FMC_HPC1_IIC_SDA		U80.12	D26	NA	NA	
C34	GA0 = 0 = GND			D27	NA	NA	
C35	VCC12_SW			D29	FMC_HPC1_TCK_BUF		U19.16
C37	VCC12_SW			D30	FPGA_TDO_FMC_TDI_BUF		U19.21
C39	UTIL_3V3			D31	FMC_HPC0_TDO_HPC1_TDI		U26.2
				D32	UTIL_3V3		
				D33	FMC_HPC1_TMS_BUF		U19.19
				D34	NA	NA	
				D35	NA		
				D36	UTIL_3V3		
				D38	UTIL_3V3		
				D40	UTIL_3V3		

Notes:
1. No I/O standards are associated with MGT connections.

Table 1-63: **J2 VITA 57.1 FMC HPC1 Sections E and F to FPGA U1 Connections**

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
E2	NA	NA		F1	FMC_HPC1_PG_M2C	LVCMOS18	BA21
E3	NA	NA		F4	NA	NA	
E6	NA	NA		F5	NA	NA	
E7	NA	NA		F7	NA	NA	

Table 1-63: **J2 VITA 57.1 FMC HPC1 Sections E and F to FPGA U1 Connections *(Cont'd)***

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
E9	NA	NA		F8	NA	NA	
E10	NA	NA		F10	NA	NA	
E12	NA	NA		F11	NA	NA	
E13	NA	NA		F13	NA	NA	
E15	NA	NA		F14	NA	NA	
E16	NA	NA		F16	NA	NA	
E18	NA	NA		F17	NA	NA	
E19	NA	NA		F19	NA	NA	
E21	NA	NA		F20	NA	NA	
E22	NA	NA		F22	NA	NA	
E24	NA	NA		F23	NA	NA	
E25	NA	NA		F25	NA	NA	
E27	NA	NA		F26	NA	NA	
E28	NA	NA		F28	NA	NA	
E30	NA	NA		F29	NA	NA	
E31	NA	NA		F31	NA	NA	
E33	NA	NA		F32	NA	NA	
E34	NA	NA		F34	NA	NA	
E36	NA	NA		F35	NA	NA	
E37	NA	NA		F37	NA	NA	
E39	VADJ_1V8_FPGA			F38	NA	NA	
				F40	VADJ_1V8_FPGA		

Table 1-64: **J2 VITA 57.1 FMC HPC1 Sections G and H to FPGA U1 Connections**

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G2	NA	NA	NA	H1	FMC_HPC1_VREF_A_M2C	NA	NA
G3	NA	NA	NA	H2	FMC_HPC1_PRSNT_M2C_B(1)	NA	AP21
G6	FMC_HPC1_LA00_CC_P	LVCMOS18	AV33	H4	FMC_HPC1_CLK0_M2C_P	LVCMOS18	AU33
G7	FMC_HPC1_LA00_CC_N	LVCMOS18	AV34	H5	FMC_HPC1_CLK0_M2C_N	LVCMOS18	AU34
G9	FMC_HPC1_LA03_P	LVCMOS18	AV36	H7	FMC_HPC1_LA02_P	LVCMOS18	AR34
G10	FMC_HPC1_LA03_N	LVCMOS18	AW36	H8	FMC_HPC1_LA02_N	LVCMOS18	AT34

Table 1-64: **J2 VITA 57.1 FMC HPC1 Sections G and H to FPGA U1 Connections *(Cont'd)***

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G12	FMC_HPC1_LA08_P	LVCMOS18	AN32	H10	FMC_HPC1_LA04_P	LVCMOS18	AP33
G13	FMC_HPC1_LA08_N	LVCMOS18	AP32	H11	FMC_HPC1_LA04_N	LVCMOS18	AR33
G15	NA	NA		H13	FMC_HPC1_LA07_P	LVCMOS18	AV35
G16	NA	NA		H14	FMC_HPC1_LA07_N	LVCMOS18	AW35
G18	NA	NA		H16	NA	NA	NA
G19	NA	NA		H17	NA	NA	
G21	NA	NA		H19	NA	NA	
G22	NA	NA		H20	NA	NA	
G24	NA	NA		H22	NA	NA	
G25	NA	NA		H23	NA	NA	
G27	NA	NA		H25	NA	NA	
G28	NA	NA		H26	NA	NA	
G30	NA	NA		H28	NA	NA	
G31	NA	NA		H29	NA	NA	
G33	NA	NA		H31	NA	NA	
G34	NA	NA		H32	NA	NA	
G36	NA	NA		H34	NA	NA	
G37	NA	NA		H35	NA	NA	
G39	VADJ_1V8_FPGA			H37	NA	NA	
				H38	NA	NA	
				H40	VADJ_1V8_FPGA		

Notes:

1. Also wired to System Controller U111.R12.

Table 1-65: **J2 VITA 57.1 FMC HPC1 Sections J and K to FPGA U1 Connections**

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
J2	NA	NA		K1	NA	NA	
J3	NA	NA		K4	NA	NA	
J6	NA	NA		K5	NA	NA	
J7	NA	NA		K7	NA	NA	
J9	NA	NA		K8	NA	NA	

Table 1-65: **J2 VITA 57.1 FMC HPC1 Sections J and K to FPGA U1 Connections *(Cont'd)***

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
J10	NA	NA		K10	NA	NA	
J12	NA	NA		K11	NA	NA	
J13	NA	NA		K13	NA	NA	
J15	NA	NA		K14	NA	NA	
J16	NA	NA		K16	NA	NA	
J18	NA	NA		K17	NA	NA	
J19	NA	NA		K19	NA	NA	
J21	NA	NA		K20	NA	NA	
J22	NA	NA		K22	NA	NA	
J24	NA	NA		K23	NA	NA	
J25	NA	NA		K25	NA	NA	
J27	NA	NA		K26	NA	NA	
J28	NA	NA		K28	NA	NA	
J30	NA	NA		K29	NA	NA	
J31	NA	NA		K31	NA	NA	
J33	NA	NA		K32	NA	NA	
J34	NA	NA		K34	NA	NA	
J36	NA	NA		K35	NA	NA	
J37	NA	NA		K37	NA	NA	
J39	NA	NA		K38	NA	NA	
				K40	NA	NA	

VCU110 Board Power System

The VCU110 hosts a Maxim PMBus based power system. Each individual Maxim MAX20751EKX or MAX15301 voltage regulator has a PMBus interface. Figure 1-29 shows the VCU110 power system block diagram.

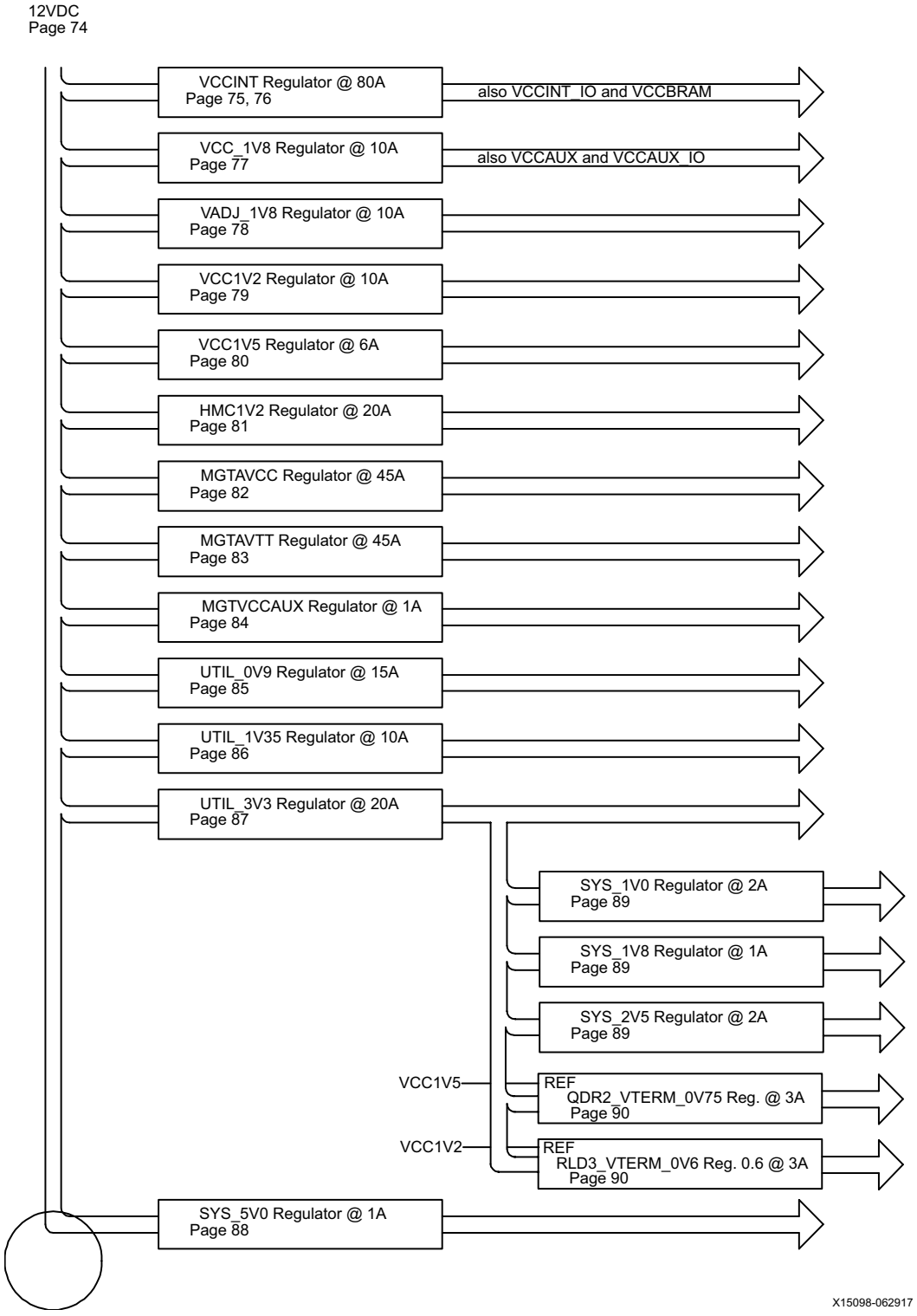

Figure 1-29: **VCU110 Power System Block Diagram**

The VCU110 evaluation board uses power regulators and PMBus compliant POL controllers from Maxim Integrated Circuits to supply the core and auxiliary voltages listed in Table 1-66.

Table 1-66: **Onboard Power System Devices**

Device Type	Reference Designator	PMBus Address	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
MAX20751EKX	U166	0x70	Maxim multiphase master with smart slaves 4xVT77518 80A	VCCINT_FPGA	0.95V	75, 76
MAX15301	U9	0x11	Maxim InTune digital POL controller 10A	VCC1V8_FPGA	1.80V	77
MAX15301	U30	0x12	Maxim InTune digital POL controller 10A	VADJ_1V8_FPGA	1.80V	78
MAX15301	U4	0x14	Maxim InTune digital POL controller 10A	VCC1V2_FPGA	1.20V	79
MAX15301	U187	0x15	Maxim InTune digital POL controller 6A	VCC1V5_FPGA	1.00V	80
MAX20751EKX	U192	0x71	Maxim multiphase master with smart slave VT1697SBFQX 20A	HMC1V2	1.20V	81
MAX20751EKX	U174	0x72	Maxim multiphase master with smart slaves VT1697SBFQX 45A	MGTAVCC_FPGA	1.00V	82
MAX20751EKX	U175	0x73	Maxim multiphase master with smart slaves VT1697SBFQX 45A	MGTAVTT_FPGA	1.20V	83
MAX20751EKX	U191	0x76	Maxim multiphase master with smart slave VT1697SBFQX 1A	MGTVCCAUX	1.80V	84
MAX20751EKX	U193	0x77	Maxim multiphase master with smart slaves VT1697SBFQX 15A	UTIL_0V9	0.90V	85
MAX15301	U150	0x1A	Maxim InTune digital POL controller 10A	UTIL_1V35	1.35V	86
MAX15301	U156	0x1B	Maxim InTune digital POL controller 20A	UTIL_3V3	3.30V	87
MAX17502	U82	NA	Maxim Adjustable Synchronous Buck Switcher 1A	SYS_5V0	5.00V	88
MAX15053	U124	NA	Maxim Adjustable Synchronous Buck Switcher 2A	SYS_1V0	1.00V	89
MAX15027	U125	NA	Maxim Adjustable LDO 1A	SYS_1V8	1.80V	89

Table 1-66: **Onboard Power System Devices *(Cont'd)***

Device Type	Reference Designator	PMBus Address	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
MAX15053	U151	NA	Maxim Adjustable Synchronous Buck Switcher 2A	SYS_2V5	2.50V	89
TPS51200	U143	NA	TI Source-Sink VTT Regulator 3A	RLD3_VTERM_0V6	0.60V	90
TPS51200	U167	NA	TI Source-Sink VTT Regulator 3A	QDR2_VTERM_0V75	0.75V	90

The VADJ_1V8_FPGA rail is programmed to 1.80V by default. This rail powers both the FMC HPC0 (J22) and FMC HPC1 (J2) V_{ADJ} pins as well as the XCVU190 HR banks 84 and 94 (refer to Table 1-3).

Documentation describing PMBUS programming for the Maxim InTune power controllers is available at the Maxim website [Ref 36].

The PCB layout and power system design meets the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 13].

Monitoring Voltage and Current

Voltage and current monitoring and control are available for the Maxim power system controllers through the Maxim PowerTool graphical user interface. The onboard Maxim InTune power controllers listed in Table 1-66 are accessed through the 2x8 keyed shrouded PMBus connector J39, which is provided for use with the Maxim PowerTool USB cable (Maxim part number MAXPOWERTOOL001#), which can be ordered from the Maxim website [Ref 36]. The associated Maxim PowerTool GUI is also downloadable from this Maxim site. This is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in Table 1-66.

SYSMON Power System Measurement

UltraScale FPGAs provide an analog front end (SYSMON) block. The SYSMON contains a single 10-bit 0.2 MSPS ADC. The VCU110 board SYSMON ADC interface includes current measuring capability for all Maxim power controller sourced rails. The Maxim PowerTool GUI can display the rail voltage for all Maxim power controller sourced rails.

V_{CCINT}, V_{CCAUX} and V_{CCBRAM} rail voltages can be displayed through the SYSMON internal voltage measurement capability.

The MGTAVCC and MGTAVTT rail voltages can be displayed through SYSMON channels AD0 and AD8, respectively.

Several rail current measurements are made available to SYSMON through an Analog Devices ADG707BRU multiplexer U75. Each Maxim controlled rail has a TI INA333 op amp strapped across a series current sense resistors' Kelvin terminals. This op amp has its gain adjusted to give 0.75V - 1V at the expected full scale current value for the rail.

Figure 1-30 shows the SYSMON external multiplexer U75 circuit block diagram.

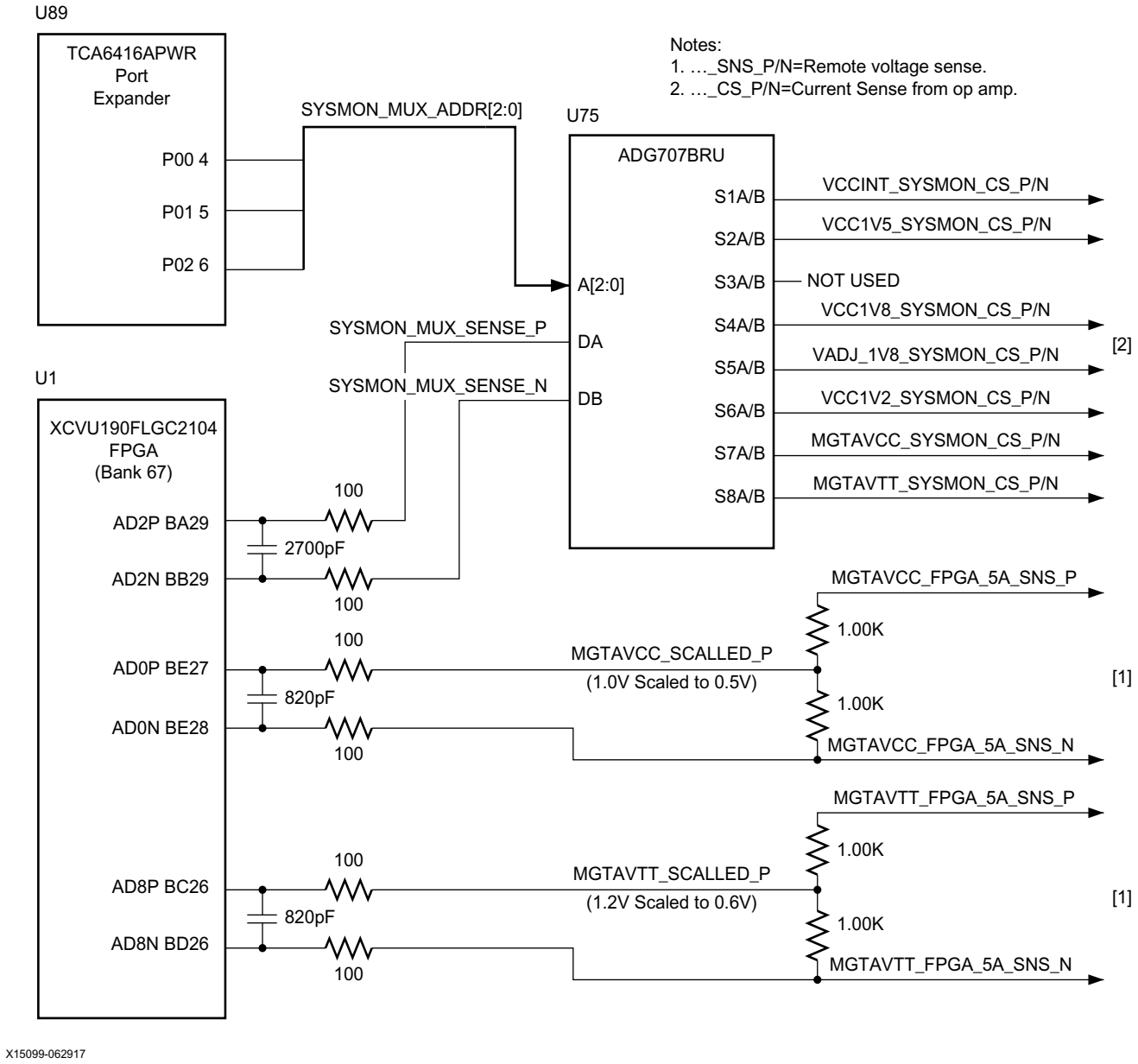

Figure 1-30: **SYSMON External Multiplexer Block Diagram**

Table 1-67 lists the VCU110 board SYSMON power system voltage and current measurement details for the external U75 MUX.

Table 1-67: **VCU110 Board SYSMON Measurements through MUX U75**

Controlled Rail Name	Regulator Type/Reference Designator	Measure V/I Type	Nominal V_{OUT}	Current Range	Isense Op Amp			Monitoring Available, Schematic Net Name	8-to-1 Mux. U75		
					Ref. Des.	Gain	V_O Range		Pin Num.	Pin Name	A[2:0]
VCCINT_FPGA	MAX20751EKX/ U166	V	0.95V	NA	NA			SYSMON or MAXIM GUI	NA		
		I	NA	0-80A 0.0005Ω	U74	15	0 - 0.95V	VCCINT_SYSMON_CS_P	19	S1A	000
								VCCINT_SYSMON_CS_N	11	S1B	
VCC1V8_FPGA	MAX15301/ U9	V	1.80V	NA	NA			SYSMON or MAXIM GUI	NA		
		I	NA	0-10A 0.005Ω	U116	20	0 - 1V	VCC1V8_SYSMON_CS_P	22	S4A	011
								VCC1V8_SYSMON_CS_N	8	S4B	
VADJ_1V8_FPGA	MAX15301/ U30	V	1.80V	NA	NA			SYSMON or MAXIM GUI	NA		
		I	NA	0-10A 0.005Ω	U119	20	0 - 1V	VADJ_1V8_SYSMON_CS_P	23	S5A	100
								VADJ_1V8_SYSMON_CS_N	7	S5B	
VCC1V2_FPGA	MAX15301/ U4	V	1.20V	NA	NA			MAXIM GUI only	NA		
		I	NA	0-10A 0.005Ω	U120	20	0 - 1V	VCC1V2_SYSMON_CS_P	24	S6A	101
								VCC1V2_SYSMON_CS_N	6	S6B	
VCC1V5_FPGA	MAX15301/ U187	V	1.50V	NA	NA			MAXIM GUI only	NA		
		I	NA	0-6A 0.005Ω	U195	30	0 - 1V	VADJ_1V5_SYSMON_CS_P	20	S2A	001
								VADJ_1V5_SYSMON_CS_N	10	S2B	
MGTAVCC_FPGA	MAX20751EKX/ U174	V	1.00V	NA	MGTAVCC_FPGA remote sense is divided to deliver 0.5V on SYSMON_AD0_R_P/N			SYSMON AD0 and MAXIM GUI	NA		
								SYSMON_AD0_R_P	FPGA U1 pin BE27		
								SYSMON_AD0_R_N	FPGA U1 pin BE28		
		I	NA	0-45A 0.001Ω	U118	20	0-1V	MGTAVCC_SYSMON_CS_P	25	S7A	110
								MGTAVCC_SYSMON_CS_N	5	S7B	
MGTAVTT_FPGA	MAX20751EKX/ U175	V	1.20V	NA	MGTAVCC_FPGA remote sense is divided to deliver 0.6V on SYSMON_AD8_R_P/N			SYSMON AD8 and MAXIM GUI	NA		
								SYSMON_AD8_R_P	FPGA U1 pin BC26		
								SYSMON_AD8_R_N	FPGA U1 pin BD26		
		I	NA	0-45A 0.001Ω	U117	20	0-1V	MGTAVCC_SYSMON_CS_P	26	S8A	111
								MGTAVCC_SYSMON_CS_N	4	S8B	

Notes:

1. MUX U75 channel S3 (address 010) is not connected.

SYSMON Headers J80, J81

UltraScale FPGAs provide an analog front end (SYSMON) block. The SYSMON contains a single 10-bit 0.2 MSPS ADC. Consequently, the sequencer for SYSMON does not support simultaneous sampling mode or independent ADC mode. See the *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 14] for details on the capabilities of the analog front end.

The VCU110 board supports both the internal FPGA sensor measurements and the external measurement capabilities of the SYSMON. Internal measurements of the die temperature, V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} are available.

The FPGA U1 bank 0 dedicated VP (FPGA U1 pin AC20) and VN (FPGA U1 pin AD19) input channel pins are dual-purpose. When pulled to GND through 20.5 kΩ resistors, the default SYSMON I2C address is set pre-configuration. The VCU110 implements 2-pin male headers (J80, J81) which can be jumpered to these pull-down resistors. The headers can be used as dedicated analog inputs post-configuration by removing the jumpers.

For external measurements, SYSMON headers (J80, J81) are provided to connect analog inputs to the FPGA VP and VN input pins. See pthe *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 14] for details.

For more detailed information about the UltraScale System Monitor (SYSMON), see *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 14].

Cooling Fan

The XCVU190 FPGA U1 cooling fan connector is shown in Figure 1-31.

The fan turns on when the VCU110 is powered on due to pull-up resistor R422. The SM_FAN_PWM and SM_FAN_TACH signals are wired to XCVU190 FPGA U1 bank 65 pins AT21 and AT19 respectively, enabling the user to implement their own fan speed control IP in the FPGA U1 logic.

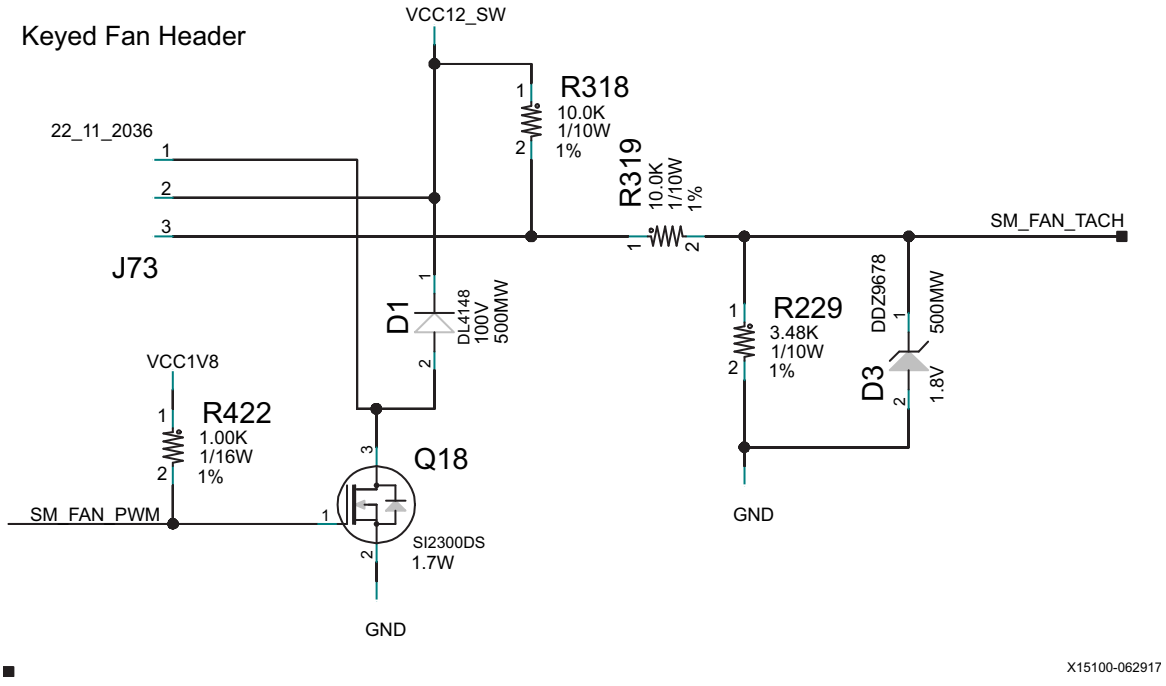

Figure 1-31: **Cooling Fan Circuit**

VCU110 Zynq-7000 SoC XC7Z010 System Controller

[Figure 1-2, callout 36]

The VCU110 XC7Z010 U111 system controller sub-system implements interfaces to:

- PMBus power system
- Programmable user clock
- Micro-SD card
- USB UART2
- Five directional user pushbutton switches
- Three GPIO connections to FPGA U1 bank 65
- IIC bus MUXes

The system controller is delivered as a black-box design that communicates with on-board programmable devices over an I2C interface. The Zynq-7000 SoC system controller IP is not provided and is not available to end users for modification purposes.

The system controller is an ease-of-use feature that sets up or queries onboard resources available to the XCVU190 UltraScale FPGA U1 on the VCU110. Programmable clocks, the internal UltraScale FPGA system monitor block (SYSMON), and the Maxim power controllers are accessible through an I2C interface connected to both the system controller and the FPGA.

A Silicon Labs Si570 programmable low-jitter clock is used to provide a system clock for FPGA designers. Through a UART (115200-8-N-1) text interface, the system clock (Si570) can be set to any frequency between 10 MHz and 810 MHz. The Si570 defaults to a power-on frequency of 156.25 MHz, but then automatically changes to the last saved frequency setting requested by the user. Clock programming does not require FPGA resources and may be set or adjusted prior to configuring the FPGA or after the FPGA has been configured.

Additional functionality provided through the system controller UART2 is a text display of the internal SYSMON registers for V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and the UltraScale FPGA U1 device temperature.

Power rail voltages set by the Maxim controllers are also displayed through the UART2 for VCCINT, VCC1V8, VADJ_1V8, VCC1V2, VCC1V5, HMC1V2, MGTAVCC, MGTAVTT, MGTVCCAUX, UTIL_0V9, UTIL_1V35, and UTIL_3V3. Refer to Table 1-66 for PMBus accessible voltage regulators.

The installation of the USB UART drivers is documented in Appendix C, Getting Started with System Controller.

AMD XILINX

Appendix A

Default Switch and Jumper Settings

The default switch and jumper settings for the VCU110 evaluation board are provided in this appendix.

Switches

Default switch settings are listed in Table A-1.

Table A-1: **Default Switch Settings**

Switch	Function	Default	Comments	Figure 1-2 Callout	Schematic 0381556 Page
SW1	SPST slide switch	Off	Board shipped with power switch off	30	71
SW12	4-pole GPIO DIP switch(1)	0000	POS 1-4 GPIO active-High	26	64
SW15	5-pole configuration DIP switch(1)	00000	POS 1-5 Zynq SoC system controller U111	28	51
SW16	3-pole configuration DIP switch(1)	101	POS 1-3 FPGA U1 mode M[2:0]	35	3

Notes:

1. DIP switches are active-High (connected net is pulled high when DIP switch is closed).

Jumpers

Default jumper positions are listed in Table A-2. See Figure A-1 for locations of jumpers listed in Table A-2.

Table A-2: **Default Jumper Settings**

Jumper	Function	Default	Comments	Figure A-1 Callout	Schematic 0381556 Page
J5	POR override	2-3	U1 POR_OVERRIDE pin P7 to GND	1	3
J12	Maxim regulator inhibit	Off	Used when programming power system	2	71
J14	U30 VADJ_1V8 enable	Off	Parallel to J12 VADJ_1V8 enable	3	74
J80	SYSMON_VP	1-2	U1 VP pin V12 pull down 20.5KΩ to GND	4	3
J81	SYSMON_VN	1-2	U1 VN pin W11 pull down 20.5KΩ to GND	4	3

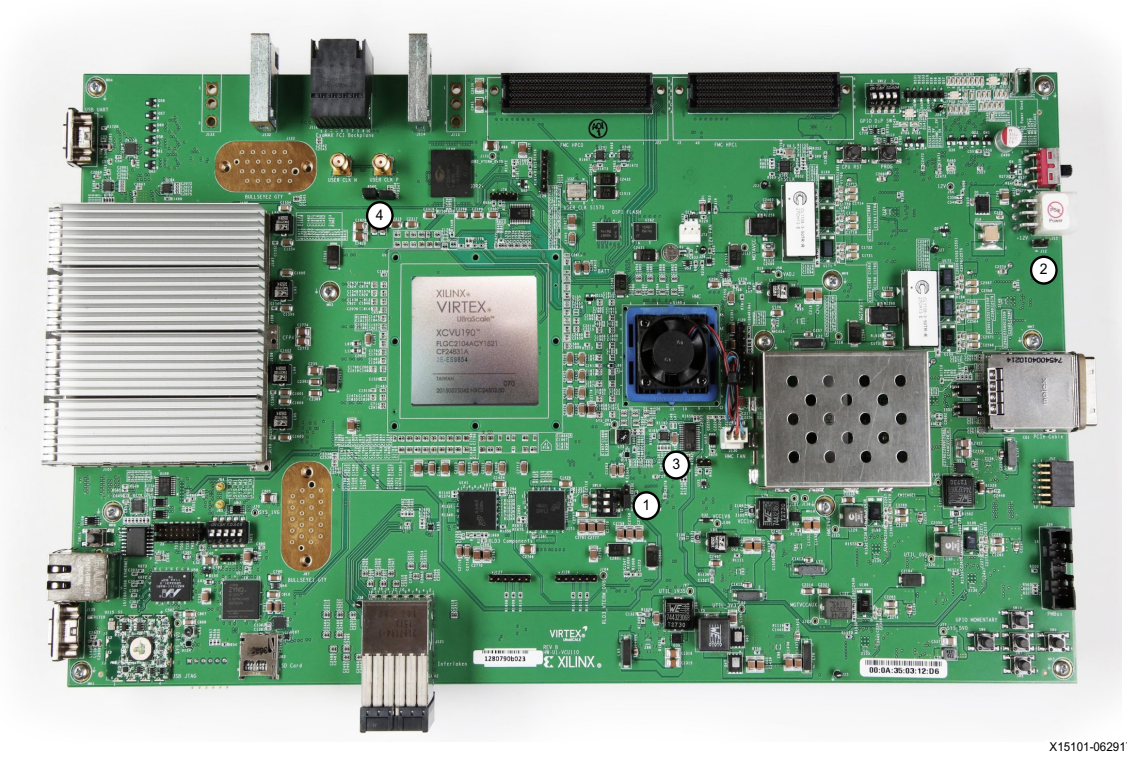

Figure A-1: **VCU110 Board Jumper Header Locations**

VITA 57.1 FMC Connector Pinouts

Overview

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) connector defined by the VITA 57.1 FMC specification. For a description of how the VCU110 evaluation board implements the FMC specification, see FPGA Mezzanine Card (FMC) Interface.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

X15102-062917

Figure B-1: **FMC HPC Connector Pinout**

Getting Started with System Controller

Overview

The Xilinx system controller is an ease-of-use application that runs at power-up on all UltraScale™ FPGA evaluation boards. These select board features can be controlled and monitored:

- Programmable clocks
- Power system monitoring (PMBus)
- UltraScale FPGA system monitor (SYSMON)
- Adjustable FMC expansion interface voltage
- GPIO pushbuttons and configuration DIP switch
- UltraScale FPGA Configuration

On power-up, the system controller presents a menu-driven selection of actions invoked by running a terminal program over a UART (115200-8-N-1) connection through the USB-to-UART bridge interface (J4) (see Figure C-1).

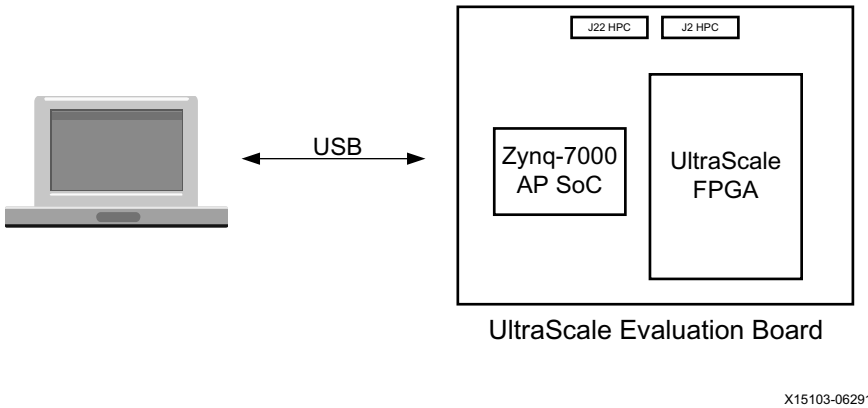

Figure C-1: **PC Host (Terminal Window) and UltraScale Evaluation Board**

To access the system controller menu:

1. Install the Silicon Labs CP2105GM dual USB-to-UART bridge driver by following the instructions in the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033) [Ref 18].
2. The Tera Term terminal application installation is referenced in the driver installation instructions in step 1, which point to the *Tera Term Terminal Emulator Installation Guide* (UG1036) [Ref 19].
3. With the VCU110 evaluation board power turned off, install the USB cable supplied in the VCU110 evaluation board kit (standard type-A end to host computer, type Micro-B end to VCU110 evaluation board connector J4).
4. Turn on the VCU110 evaluation board. The PC recognizes that new hardware is connected, and runs the driver installation wizard to complete the installation of the CP2015GM bridge chip drivers. The system controller UART appears in the PC device manager ports (COM &LPT) list as the Silicon Labs Dual CP210x Enhanced COM Port (COMnn).
5. Open a Tera Term terminal window on the PC desktop. In the New connection dialog box, click the serial radio button, and then click the drop-down arrow to open the list of ports. Select the COM port with the Enhanced description. Click OK.
6. At the top of the Tera Term VT window, select Setup > Serial port. In the dialog box that appears, set baud rate to 115200, data to 8 bit, parity to none, stop to 1 bit, and flow control to none. Click OK.
7. Power cycle the VCU110 evaluation board. The Tera Term window displays the VCU110 evaluation board system controller main menu. The main menu lists sub-menus that carry out selected actions.

```
VCU110 System Controller
- Clock Menu-
1. Set VCU110 Si570 User Clock Frequency
2. Set VCU110 Si5328 CFP4 Clock Frequency
3. Set VCU110 Si5328 ILKN & EXAMAX Frequency
4. Set VCU110 Si5328 HMC MEM & FPGA Frequency
5. Set VCU110 Si5328 HMC 15G Frequency (MEM=125 MHz, FPGA=187.5 MHz)
6. Set VCU110 Si5328 HMC 12.5G, 10G Frequency (MEM=125 MHz, FPGA=125 MHz)
7. Set VCU110 Si5328 HMC 12.5G, 10G Frequency (MEM=156.25 MHz, FPGA=156.25 MHz)
8. Save VCU110 Clock Frequency to EEPROM
9. Restore VCU110 Clock Frequency from EEPROM
A. View VCU110 Saved Clocks in EEPROM
B. Set VCU110 Clock Restore Options
C. Read VCU110 Si570 User Clock Frequency
D. Read VCU110 Si5328 MGT Clock Frequency
0. Return to Main Menu
Select an option
```

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Appendix D

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the VCU110 board provides for designs targeting the VCU110 evaluation board. Net names in the constraints file correlate with net names on the latest VCU110 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 15] for more information.

The FMC connectors J22 (HPC0) and J2 (HPC1) are connected to 1.8V VADJ banks. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT: *The VCU110 XDC file can be found on the Documentation tab (Board Files checkbox, files associated with VCU110 Schematics) of the Xilinx Virtex UltraScale FPGA VCU110 Development Kit website.*

Board Setup

See the *VCU110 Board Interface Test Tutorial* (XTP373) on the Xilinx Virtex UltraScale FPGA VCU110 Development Kit product page to get started using the evaluation board. This tutorial provides instructions for setting up the board to test all the internal and external board interfaces.

Board Specifications

Dimensions

Height: 8.50 inches (21.590 centimeters)
Thickness (± 10%): 0.150 inch (0.381 cm)
Length: 14.45 inches (36.7 centimeters)

Environmental

Temperature

Operating: 0°C to +45°C
Storage: –25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

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Appendix G

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the VCU110 board master answer record concerning the CE requirements for the PC Test Environment: VCU110 Evaluation Kit Master Answer Record 62604

The Virtex UltraScale VCU110 Declaration of Conformity is online.

CE Directives

2006/95/EC, Low Voltage Directive (LVD)

2004/108/EC, Electromagnetic Compatibility (EMC) Directive

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

IMPORTANT: *This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.*

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

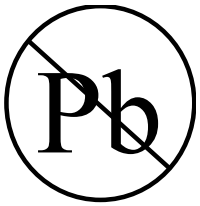
EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.



This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

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Appendix H

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see: Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the VCU110 board and its documentation is available on the following websites.

Virtex UltraScale FPGA VCU110 Development Kit

VCU110 Evaluation Kit Master Answer Record 62604

These Xilinx documents provide supplemental material useful with this guide:

1. *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893)
2. *UltraScale Architecture Configuration User Guide* (UG570)
3. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
4. *UltraScale Architecture Clocking Resources User Guide* (UG572)
5. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
6. *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182)
7. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
8. *UltraScale Devices Gen 3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156)
9. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
10. *AXI UART Lite LogiCORE IP Product Guide* (PG142)
11. *Zynq-7000 SoC Data Sheet: Overview* (DS190)
12. *Zynq-7000 SoC Technical Reference Manual* (UG585)
13. *UltraScale Architecture PCB Design User Guide* (UG583)
14. *UltraScale Architecture System Monitor User Guide* (UG580)
15. *Vivado Design Suite User Guide: Using Constraints* (UG903)
16. *Zynq-7000 SoC PCB Design Guide* (UG933)
17. *Zynq-7000 SoC Packaging and Pinout Product Specification* (UG865)
18. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
19. Tera Term Terminal Emulator Installation Guide (UG1036)

For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

The following websites provide supplemental material useful with this guide:

20. Cypress Semiconductor: www.cypress.com (CY7C2663KV18-550BZXC)
21. Micron Technology: www.micron.com (MT44K16M36RB-093E, MT44K32M18RB-093E, MT43A4G40200NFA, N25QU512ABA8E12-0SIT)
22. SanDisk: www.sandisk.com
23. SD Association: www.sdcard.org
24. Digilent: www.digilentinc.com (USB JTAG Module, Pmod Peripheral Modules)
25. Silicon Labs: www.silabs.com (Si5335A, Si570, Si53340, Si5328C)
26. PCI Express® standard: www.pcisig.com/specifications
27. SFF-8663 specification: ftp.seagate.com/sff
28. CFP MSA Hardware Specification: www.cfp-msa.org
29. Marvell Semiconductor: www.marvell.com and www.marvel.com/transceivers/alaska-gbe (88E1111)
30. Analog Devices: www.analog.com/en/index.html (ADV7511KSTZ-P, ADP123)
31. Texas Instruments: www.ti.com (TCA9548, PCA9544, TCA6416)
32. Sourcegate Technologies: www.sourcegate.net/home/

    The Xilinx board ATX-to-Mini-Fit cable, Xilinx part number 2600304, is manufactured for Xilinx by Sourcegate Technologies.

    Sourcegate Technologies part number AZCBL-WH-11009. Sourcegate only manufactures the latest revision, which is A4.

    Contact Aries Ang, aries.ang@sourcegate.net, +65 6483 2878 for price and availability. This is a custom cable and the Sourcegate website cannot be used for ordering (contact Aries Ang directly).

33. Interlaken Alliance: www.interlakenalliance.com
34. Samtec Inc.: www.samtec.com (SEAF series connectors)
35. VITA FMC Marketing Alliance: www.vita.com (FPGA Mezzanine Card (FMC) VITA 57.1 specification)
36. Maxim InTune Digital PowerTool Software Version 1.06.09 is available. Create a Maxim account and login first: www.maximintegrated.com/products/power/intune
37. IEEE Standard 802.3-2005: standards.ieee.org/getieee802

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/27/2023	1.6	Correction to board model in References. General updates.
04/19/2019	1.5	Added Electrostatic Discharge Caution. Updated component information in QDR2+ Component Memory and RLD3 Component Memory. Removed the constraints file in Appendix D, Xilinx Design Constraints and added instructions to access the file. Updated Appendix G, Regulatory and Compliance Information.
07/28/2017	1.4	Updated the UltraScale XCVU190-2FLGC2104EES9847 FPGA part number to XCVU190-2FLGC2104E throughout. Standardized figure format. Added Documentation Navigator and Design Hubs.
03/15/2017	1.3	Updated Micron HMC part number throughout. Updated Table 1-16, Table 1-18, Table 1-51, and Table 1-52.
03/26/2016	1.2	Updated Dual Quad-SPI Flash Memory, Micro-SD Card Interface, and FMC HPC1 Connector J2. Updated Table 1-15, Table 1-16, Table 1-17, Table 1-18, Table 1-19, Table 1-20, Table 1-23, Table 1-24, Table 1-25, Table 1-40, and Table 1-59. Added thickness information to Appendix F, Board Specifications.
01/16/2016	1.1	Updated the UltraScale XCVU190-2FLGC2104EES9847 FPGA part number throughout.
11/21/2015	1.0	Initial Xilinx release.

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